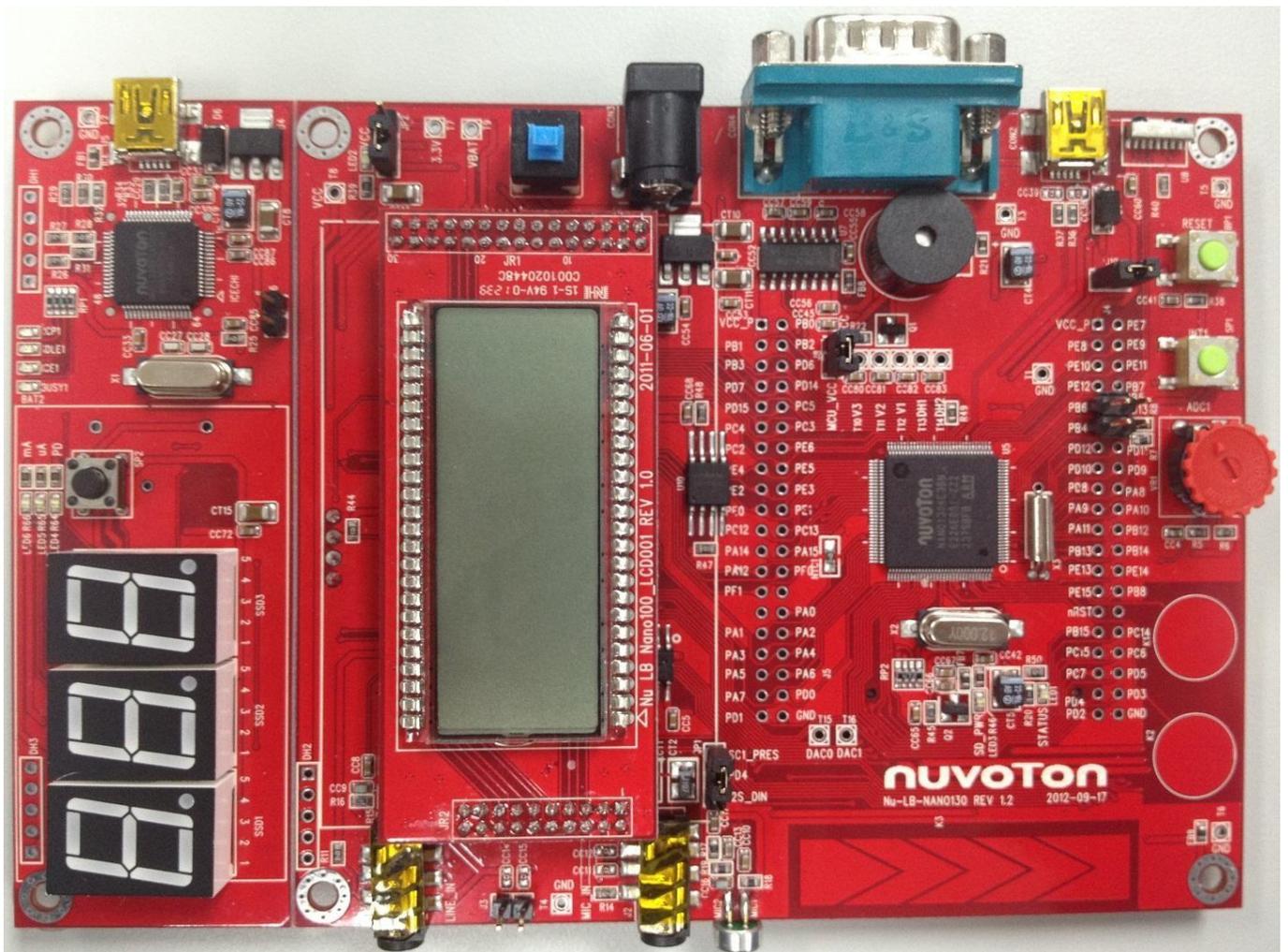


## HƯỚNG DẪN SỬ DỤNG KIT NU-LB-Nano130



## MỤC LỤC

<b>MỤC LỤC</b> .....	<b>2</b>
<b>1. Giới thiệu dòng Nano100Series</b> .....	<b>3</b>
1.1 Nano100 Series family .....	3
1.2 Các đặc điểm dòng Nano100 Series.....	4
<b>2. BOARD NU-LB-Nano130</b> .....	<b>5</b>
2.1 Giao tiếp LCD .....	7
2.1.1 Board LCD glass 4x40 .....	7
2.1.2 TFT LCD Board(GFT024CA240320).....	8
2.2 Giao tiếp với thẻ nhớ SD/MMC .....	9
2.3 Giao tiếp với Smart Card SMC .....	10
2.4 Giao tiếp I2C với EEPROM (24LC64).....	10
2.5 Giao tiếp SPI với bộ nhớ FLASH (W25Q16LC).....	11
2.6 Giao tiếp UART .....	11
2.7 Giao tiếp hồng ngoại IrDA (HSDL-3201) .....	12
2.8 Giao tiếp USB .....	12
2.9 Giao tiếp cảm ứng điện dung (Touch Key).....	13
2.10 Giao tiếp Audio (I2S).....	14
<b>3. Chân cắm mở rộng và bảng chức năng các chân I/O</b> .....	<b>15</b>
3.1 Chân cắm mở rộng .....	15
3.2 Bảng chức năng các chân I/O .....	15
<b>4. Nguồn và các Jăm nối</b> .....	<b>38</b>
<b>5. Sơ đồ mạch nguyên lý</b> .....	<b>40</b>
<b>6. Công cụ hỗ trợ lập trình và phát triển</b> .....	<b>51</b>
6.1 Công cụ hỗ trợ.....	51
6.2 Bổ sung và chỉnh sửa tài liệu .....	57
<b>7. Lập trình Nano100 Series</b> .....	<b>69</b>
7.1 Giao tiếp LCD .....	70
7.2 Giao tiếp Touch Key .....	74

## 1. Giới thiệu dòng Nano100Series

### 1.1 Nano100 Series family

Nano100 Series gồm 4 dòng:

- ✓ Nano100 Base Line : Dòng cơ bản
- ✓ Nano110 LCD Line : Ngoài tính năng cơ bản, có hỗ trợ giao tiếp LCD
- ✓ Nano120 USB Connectivity Line : Hỗ trợ giao tiếp USB
- ✓ Nano130 Advanced Line : Hỗ trợ đầy đủ các tính năng dòng Nano100 Series

#### Dòng Nano100 Base Line

Part No.	Flash	SRAM	Data Flash Shared AP ROM	LDRROM ISP Flash	I/O	Timer	Connectivity				I2S	PWM	12-bit ADC	RTC	EBI	IRC 10KHz 12MHz	PDMA	LCD	12-bit DAC	Smart Card	Touch Key	ISP ICP	Package
							UART	SPI	I2C	USB													
NANO100LC2BN	32K	8K	Configurable	4K	up to 38	4x32-bit	4	3	2	-	1	6	7	V	-	V	8	-	2	2	4	V	LQFP48
NANO100LD2BN	64K	8K	Configurable	4K	up to 38	4x32-bit	4	3	2	-	1	6	7	V	-	V	8	-	2	2	4	V	LQFP48
NANO100LD3BN	64K	16K	Configurable	4K	up to 38	4x32-bit	4	3	2	-	1	6	7	V	-	V	8	-	2	2	4	V	LQFP48
NANO100LE3BN	128K	16K	Configurable	4K	up to 38	4x32-bit	4	3	2	-	1	6	7	V	-	V	8	-	2	2	4	V	LQFP48
NANO100SC2BN	32K	8K	Configurable	4K	up to 52	4x32-bit	5	3	2	-	1	8	7	V	-	V	8	-	2	3	8	V	LQFP64
NANO100SD2BN	64K	8K	Configurable	4K	up to 52	4x32-bit	5	3	2	-	1	8	7	V	-	V	8	-	2	3	8	V	LQFP64
NANO100SD3BN	64K	16K	Configurable	4K	up to 52	4x32-bit	5	3	2	-	1	8	7	V	-	V	8	-	2	3	8	V	LQFP64
NANO100SE3BN	128K	16K	Configurable	4K	up to 52	4x32-bit	5	3	2	-	1	8	7	V	-	V	8	-	2	3	8	V	LQFP64
NANO100KC2BN	32K	8K	Configurable	4K	up to 86	4x32-bit	5	3	2	-	1	8	12	V	V	V	8	-	2	3	16	V	LQFP128
NANO100KD2BN	64K	8K	Configurable	4K	up to 86	4x32-bit	5	3	2	-	1	8	12	V	V	V	8	-	2	3	16	V	LQFP128
NANO100KD3BN	64K	16K	Configurable	4K	up to 86	4x32-bit	5	3	2	-	1	8	12	V	V	V	8	-	2	3	16	V	LQFP128
NANO100KE3BN	128K	16K	Configurable	4K	up to 86	4x32-bit	5	3	2	-	1	8	12	V	V	V	8	-	2	3	16	V	LQFP128

#### Dòng Nano110 LCD Line

Part No.	Flash	SRAM	Data Flash Shared AP ROM	LDRROM ISP Flash	I/O	Timer	Connectivity				I2S	PWM	12-bit ADC	RTC	EBI	IRC 10KHz 12MHz	PDMA	LCD	12-bit DAC	Smart Card	Touch Key	ISP ICP	Package
							UART	SPI	I2C	USB													
NANO110SC2BN	32K	8K	Configurable	4K	up to 51	4x32-bit	5	3	2	-	1	7	7	V	-	V	8	4x31, 6x29	2	3	8	V	LQFP64
NANO110SD2BN	64K	8K	Configurable	4K	up to 51	4x32-bit	5	3	2	-	1	7	7	V	-	V	8	4x31, 6x29	2	3	8	V	LQFP64
NANO110SD3BN	64K	16K	Configurable	4K	up to 51	4x32-bit	5	3	2	-	1	7	7	V	-	V	8	4x31, 6x29	2	3	8	V	LQFP64
NANO110SE3BN	128K	16K	Configurable	4K	up to 51	4x32-bit	5	3	2	-	1	7	7	V	-	V	8	4x31, 6x29	2	3	8	V	LQFP64
NANO110KC2BN	32K	8K	Configurable	4K	up to 86	4x32-bit	5	3	2	-	1	8	12	V	V	V	8	4x40, 6x38	2	3	16	V	LQFP128
NANO110KD2BN	64K	8K	Configurable	4K	up to 86	4x32-bit	5	3	2	-	1	8	12	V	V	V	8	4x40, 6x38	2	3	16	V	LQFP128
NANO110KD3BN	64K	16K	Configurable	4K	up to 86	4x32-bit	5	3	2	-	1	8	12	V	V	V	8	4x40, 6x38	2	3	16	V	LQFP128
NANO110KE3BN	128K	16K	Configurable	4K	up to 86	4x32-bit	5	3	2	-	1	8	12	V	V	V	8	4x40, 6x38	2	3	16	V	LQFP128

#### Dòng Nano120 USB Line

Part No.	Flash	SRAM	Data Flash Shared AP ROM	LDRROM ISP Flash	I/O	Timer	Connectivity				I2S	PWM	12-bit ADC	RTC	EBI	IRC 10KHz 12MHz	PDMA	LCD	12-bit DAC	Smart Card	Touch Key	ISP ICP	Package
							UART	SPI	I2C	USB													
NANO120LC2BN	32K	8K	Configurable	4K	up to 34	4x32-bit	4	3	2	1	1	4	7	V	-	V	8	-	2	2	4	V	LQFP48
NANO120LD2BN	64K	8K	Configurable	4K	up to 34	4x32-bit	4	3	2	1	1	4	7	V	-	V	8	-	2	2	4	V	LQFP48
NANO120LD3BN	64K	16K	Configurable	4K	up to 34	4x32-bit	4	3	2	1	1	4	7	V	-	V	8	-	2	2	4	V	LQFP48
NANO120LE3BN	128K	16K	Configurable	4K	up to 34	4x32-bit	4	3	2	1	1	4	7	V	-	V	8	-	2	2	4	V	LQFP48
NANO120SC2BN	32K	8K	Configurable	4K	up to 48	4x32-bit	5	3	2	1	1	8	7	V	-	V	8	-	2	3	8	V	LQFP64
NANO120SD2BN	64K	8K	Configurable	4K	up to 48	4x32-bit	5	3	2	1	1	8	7	V	-	V	8	-	2	3	8	V	LQFP64
NANO120SD3BN	64K	16K	Configurable	4K	up to 48	4x32-bit	5	3	2	1	1	8	7	V	-	V	8	-	2	3	8	V	LQFP64
NANO120SE3BN	128K	16K	Configurable	4K	up to 48	4x32-bit	5	3	2	1	1	8	7	V	-	V	8	-	2	3	8	V	LQFP64
NANO120KC2BN	32K	8K	Configurable	4K	up to 86	4x32-bit	5	3	2	1	1	8	8	V	V	V	8	-	2	3	8	V	LQFP128
NANO120KD2BN	64K	8K	Configurable	4K	up to 86	4x32-bit	5	3	2	1	1	8	8	V	V	V	8	-	2	3	16	V	LQFP128
NANO120KD3BN	64K	16K	Configurable	4K	up to 86	4x32-bit	5	3	2	1	1	8	8	V	V	V	8	-	2	3	16	V	LQFP128
NANO120KE3BN	128K	16K	Configurable	4K	up to 86	4x32-bit	5	3	2	1	1	8	8	V	V	V	8	-	2	3	16	V	LQFP128

#### Dòng Nano130 Advanced Line

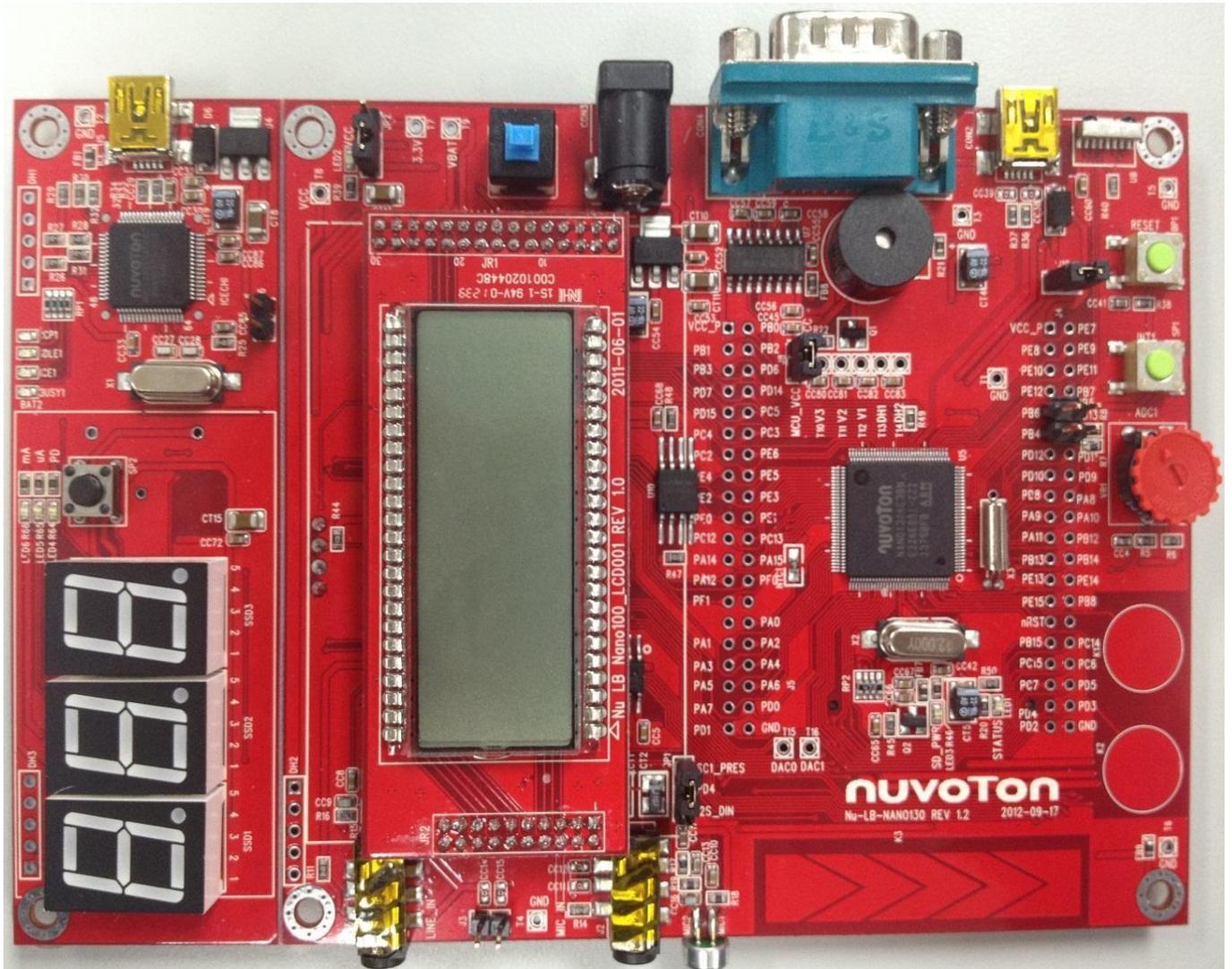
Part No.	Flash	SRAM	Data Flash Shared AP ROM	LDRROM ISP Flash	I/O	Timer	Connectivity				I2S	PWM	12-bit ADC	RTC	EBI	IRC 10KHz 12MHz	PDMA	LCD	12-bit DAC	Smart Card	Touch Key	ISP ICP	Package
							UART	SPI	I2C	USB													
NANO130SC2BN	32K	8K	Configurable	4K	up to 47	4x32-bit	5	3	2	1	1	7	7	V	-	V	8	4x31, 6x29	2	3	8	V	LQFP64
NANO130SD2BN	64K	8K	Configurable	4K	up to 47	4x32-bit	5	3	2	1	1	7	7	V	-	V	8	4x31, 6x29	2	3	8	V	LQFP64
NANO130SD3BN	64K	16K	Configurable	4K	up to 47	4x32-bit	5	3	2	1	1	7	7	V	-	V	8	4x31, 6x29	2	3	8	V	LQFP64
NANO130SE3BN	128K	16K	Configurable	4K	up to 47	4x32-bit	5	3	2	1	1	7	7	V	-	V	8	4x31, 6x29	2	3	8	V	LQFP64
NANO130KC2BN	32K	8K	Configurable	4K	up to 86	4x32-bit	5	3	2	1	1	8	8	V	V	V	8	4x40, 6x38	2	3	16	V	LQFP128
NANO130KD2BN	64K	8K	Configurable	4K	up to 86	4x32-bit	5	3	2	1	1	8	8	V	V	V	8	4x40, 6x38	2	3	16	V	LQFP128
NANO130KD3BN	64K	16K	Configurable	4K	up to 86	4x32-bit	5	3	2	1	1	8	8	V	V	V	8	4x40, 6x38	2	3	16	V	LQFP128
NANO130KE3BN	128K	16K	Configurable	4K	up to 86	4x32-bit	5	3	2	1	1	8	8	V	V	V	8	4x40, 6x38	2	3	16	V	LQFP128

### 1.2 Các đặc điểm dòng Nano100 Series

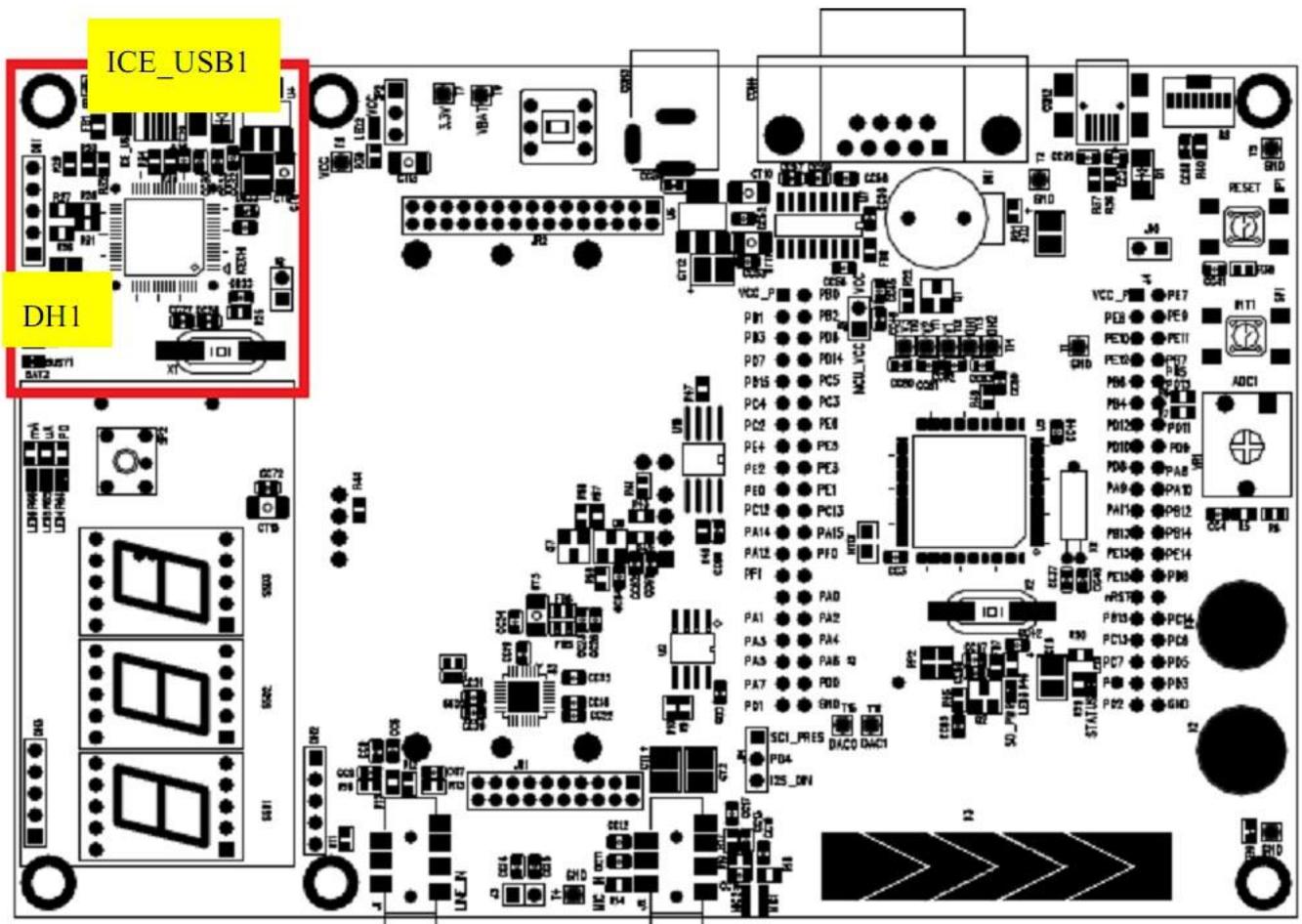
Dòng Nano130 là mang đầy đủ tính năng của dòng Nano100 Series:

- ✓ Dải điện áp hoạt động thấp: 1.8 ~ 3.6VDC
- ✓ Tần số CPU lên tới 42Mhz
- ✓ Hỗ trợ nạp ICP/ISP
- ✓ 32/64/128K Bytes bộ nhớ Flash
- ✓ 8/16K Bytes bộ nhớ SRAM
- ✓ Nhiều chân vào ra số
- ✓ 8 kênh ADC 12 bits
- ✓ 2 kênh DAC 12 bits
- ✓ Các khối giao tiếp: 2xUART, IrDA, 2xSPI, 2xI2C, I2S, USB...
- ✓ Khối điều khiển động cơ 8xPWM ✓RTC
- ✓ Hỗ trợ giao tiếp LCD 4x40 hoặc 6x38
- ✓ Hỗ trợ giao tiếp cảm ứng điện dung(Touch key)
- ✓ Hỗ trợ giao tiếp Smart Card : 3xISO-7816-3

## 2. BOARD NU-LB-Nano130



Hình 2.1 NU-LB-Nano130 Board



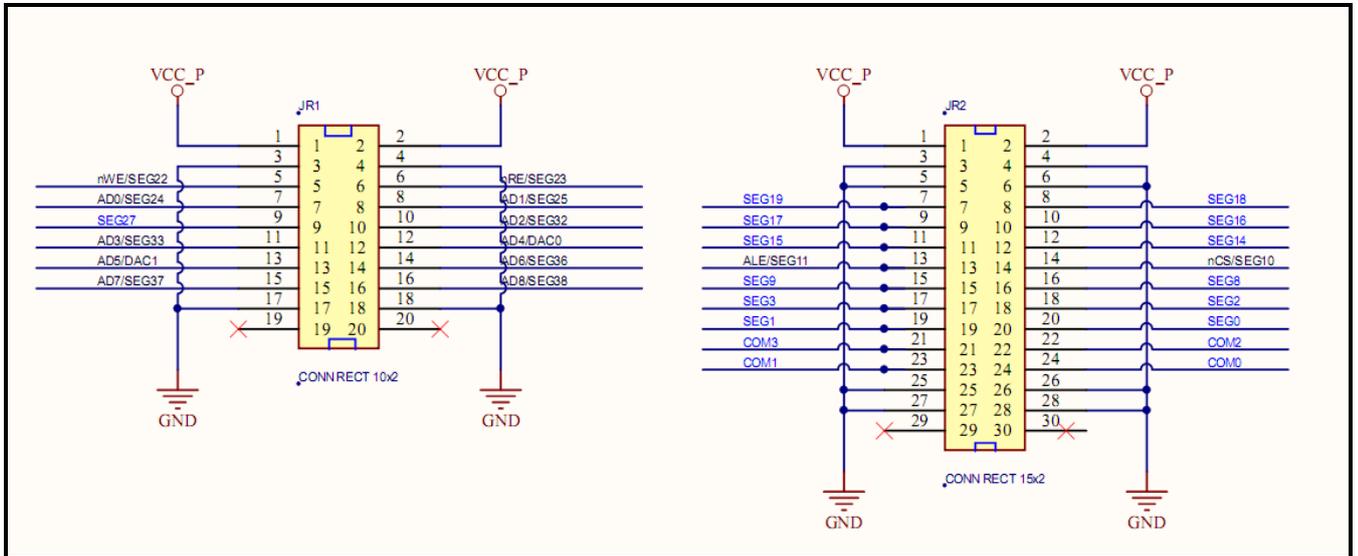
Hình 2.2 NU-LB-Nano130 PCB

Các thành phần chính:

1. **MCU:** Nano130KE3BN
2. **AUDIO:** WAU8822 audio codec
3. **I2C EEPROM:** giao tiếp với 24LC64
4. **SPI FLASH:** 25Q16 SPI serial FLASH
5. **UART:** Kết nối máy tính qua cổng UART Port0
6. **Khe cắm SD card:** Giao tiếp SPI với thẻ nhớ MMC/SD
7. **Khe cắm Smart card:** Giao tiếp qua cổng SMC Port1
8. **Mạch nạp ICE-USB**
9. **LCD connector:** Hỗ trợ moduel TN/STN LCD và TFT LCM
10. **Touch Pads:** 5-key slider và 2 key touch pads
11. **ADC, Buzz, Led 7 thanh.**
12. **Giắc nguồn DC**

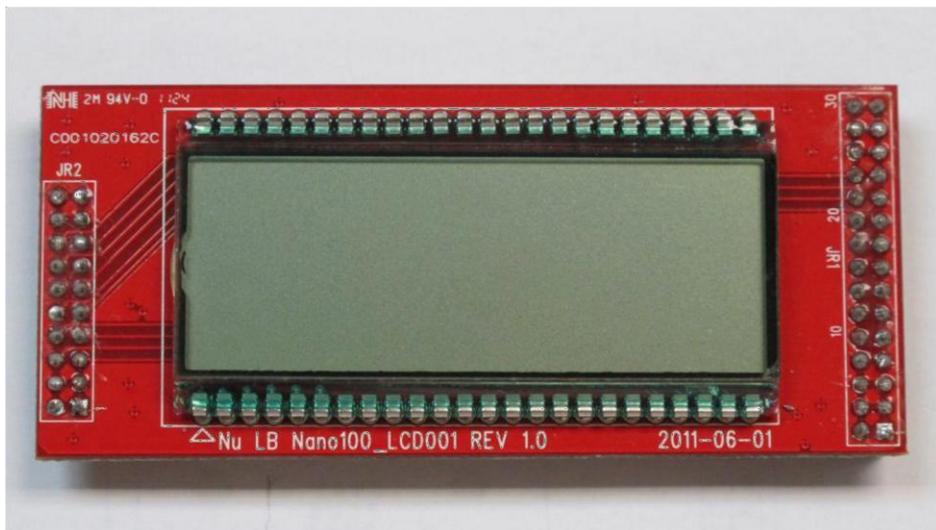
## 2.1 Giao tiếp LCD

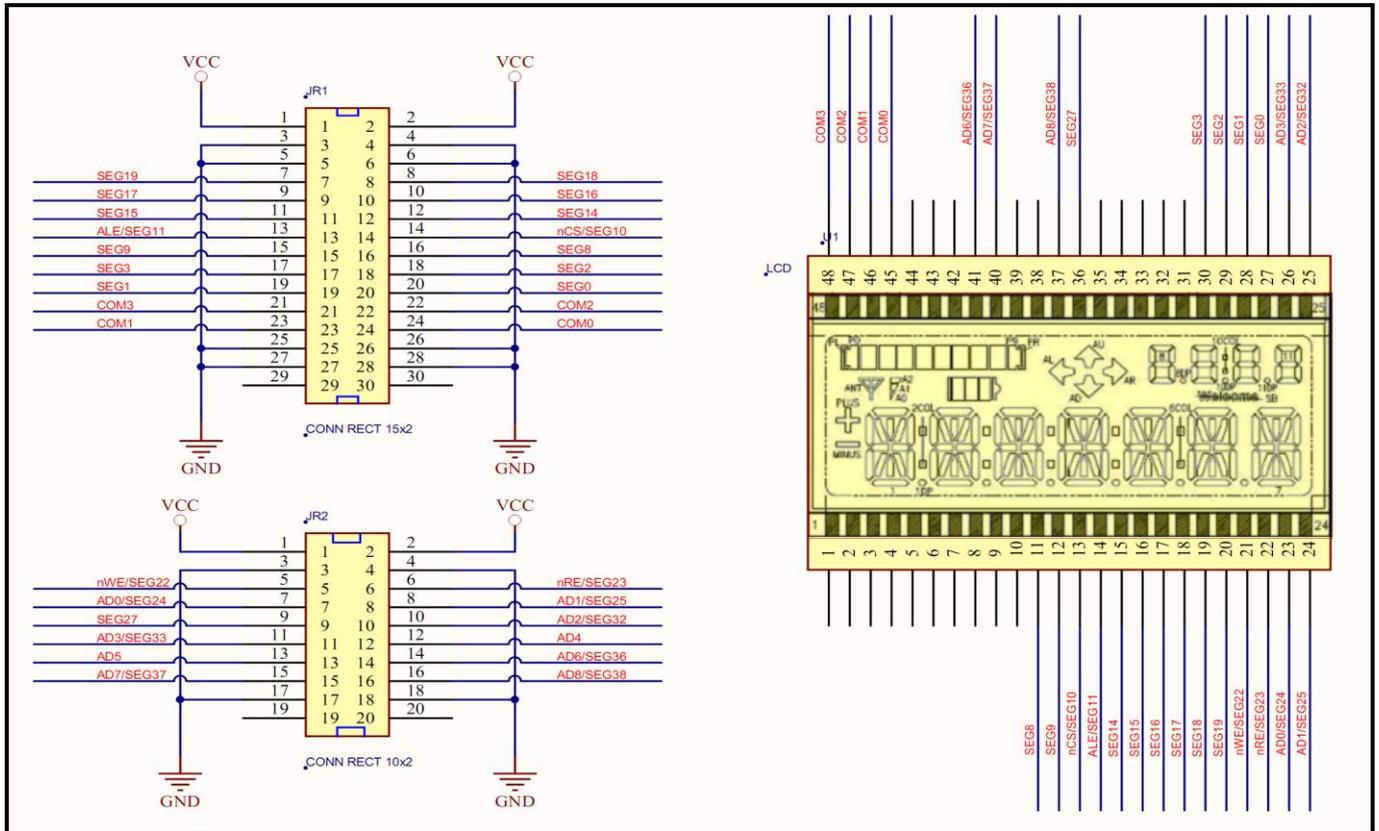
Kit NU-LB-Nano130 có sẵn connector, kết nối với module LCD glass và TFT LCD 240x320 (GFT024CA240320)



Hình 2.3 Connector kết nối LCD

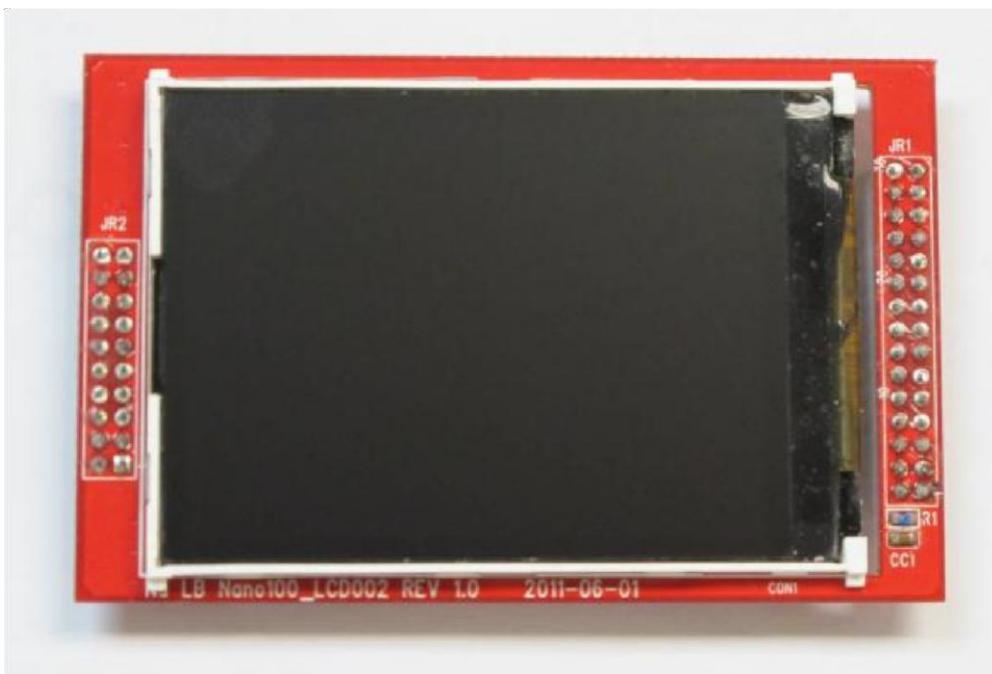
### 2.1.1 Board LCD glass 4x40

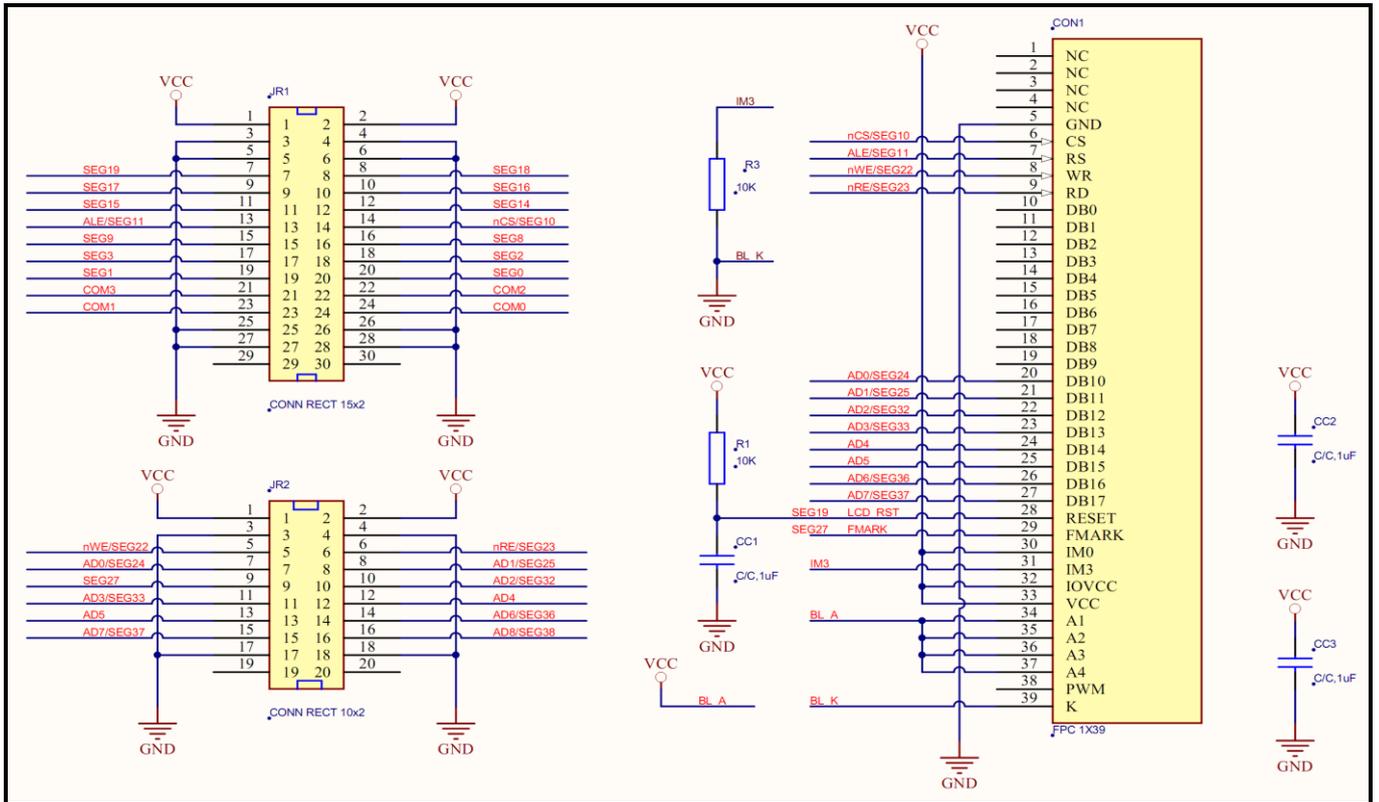




Hình 2.4 LCD glass 4x40

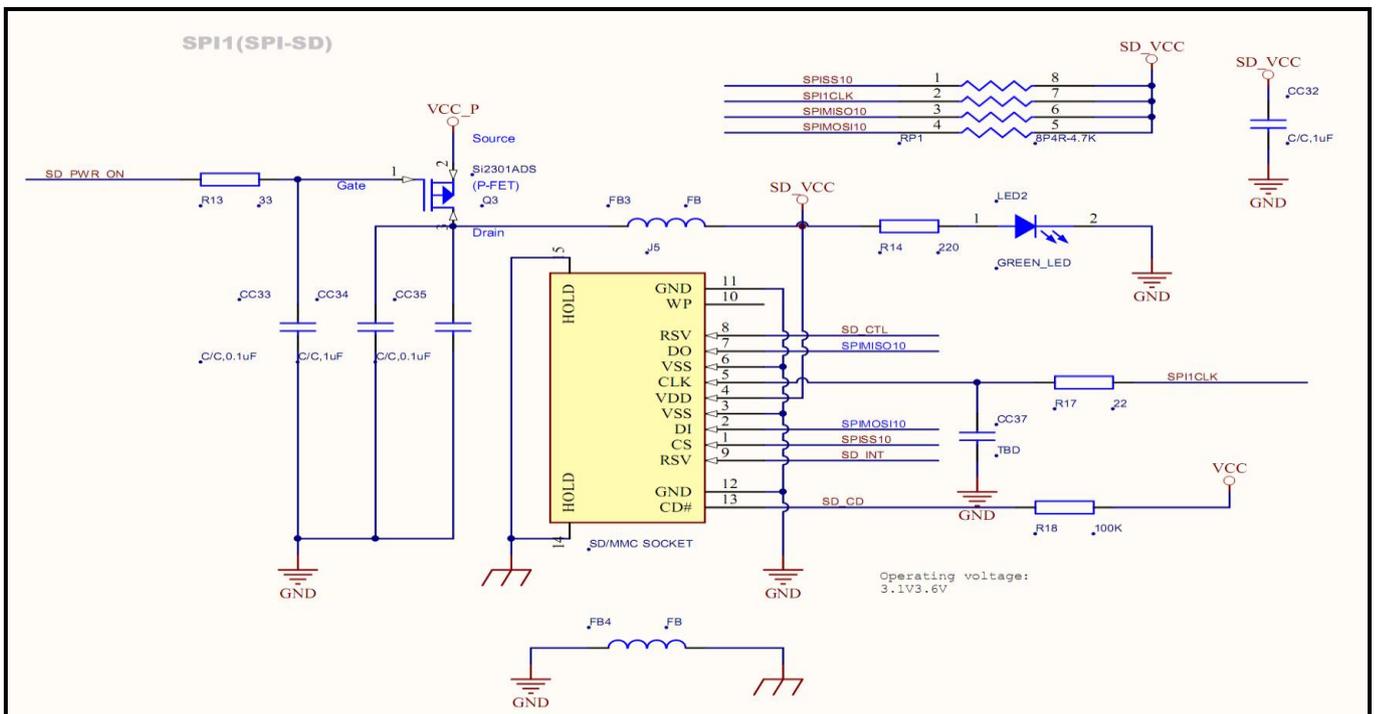
### 2.1.2 TFT LCD Board(GFT024CA240320)





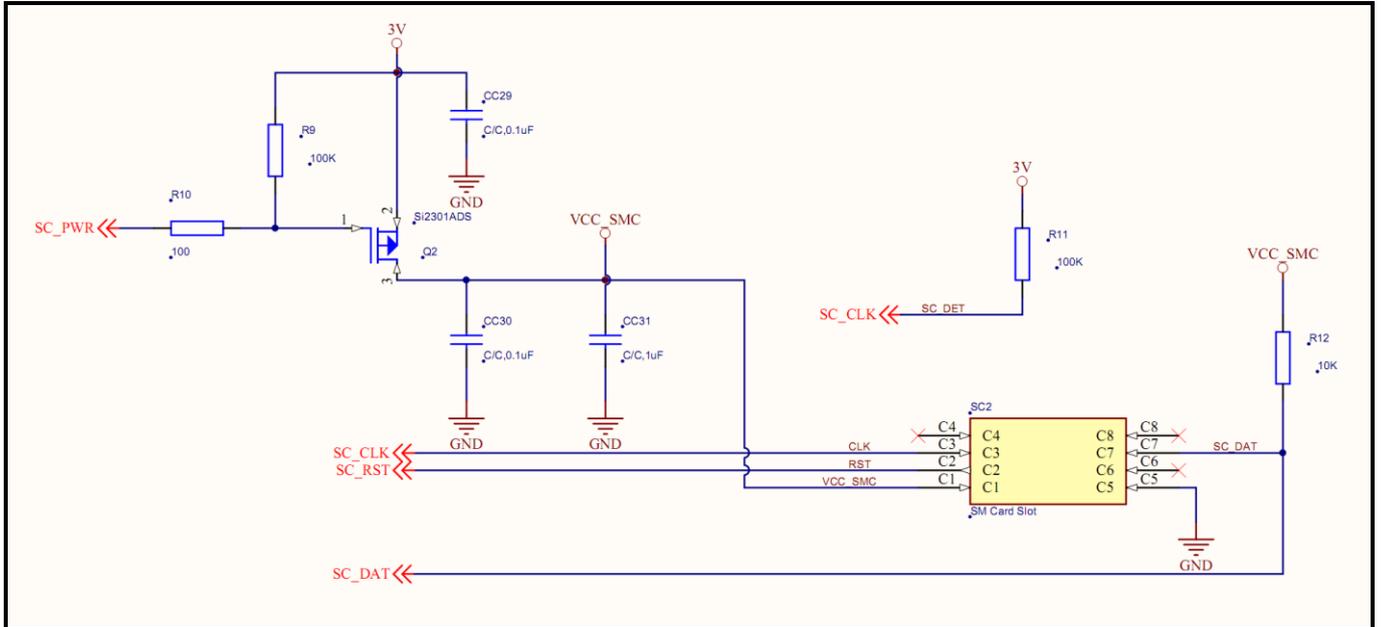
Hình 2.5 TFT LCD GFT024CA240320

## 2.2 Giao tiếp với thẻ nhớ SD/MMC



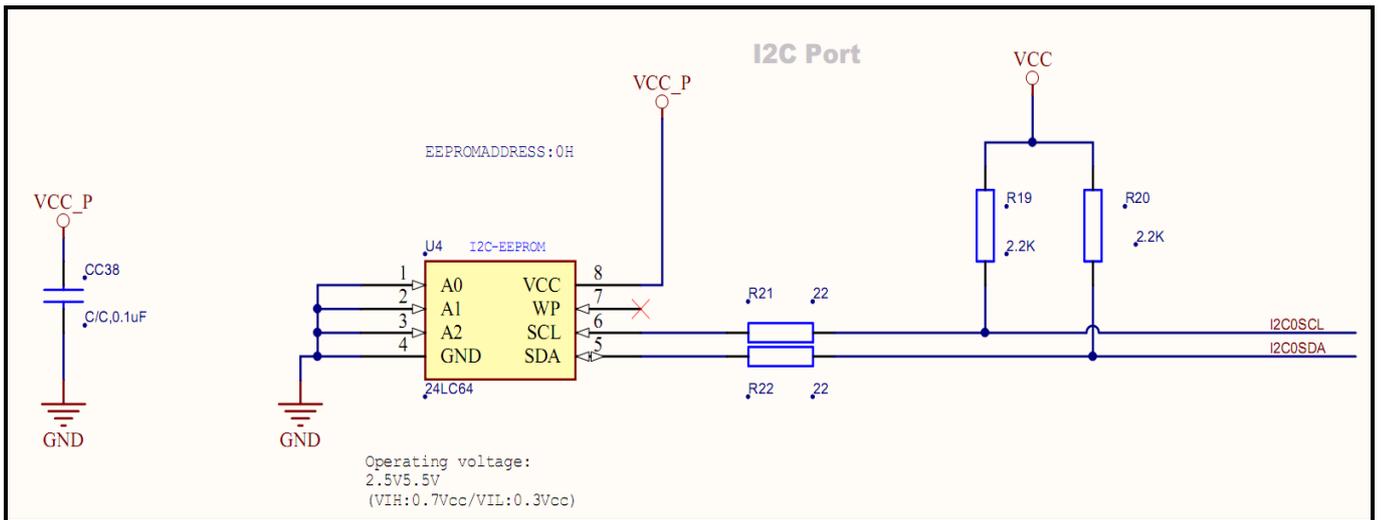
Hình 2.6 Giao tiếp SD/MMC Card

### 2.3 Giao tiếp với Smart Card SMC



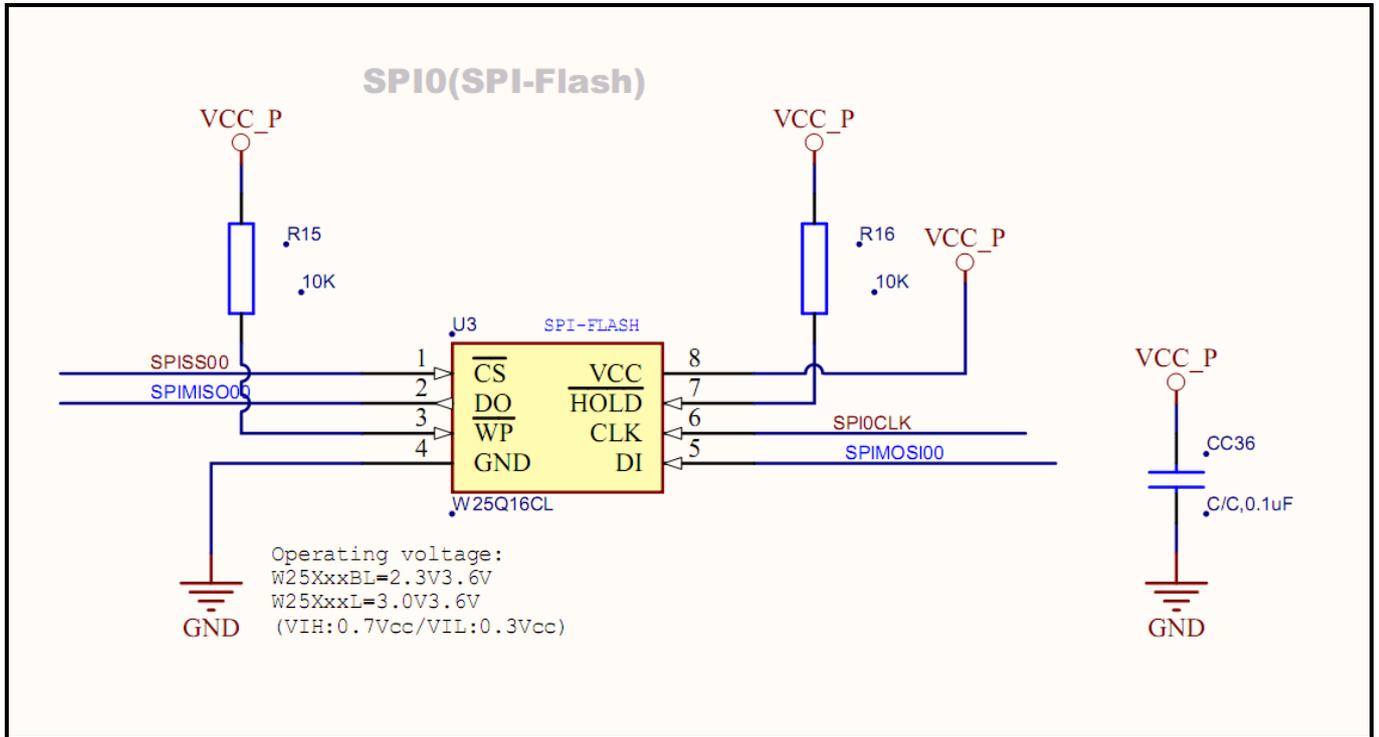
Hình 2.7 Giao tiếp Smart Card

### 2.4 Giao tiếp I2C với EEPROM (24LC64)



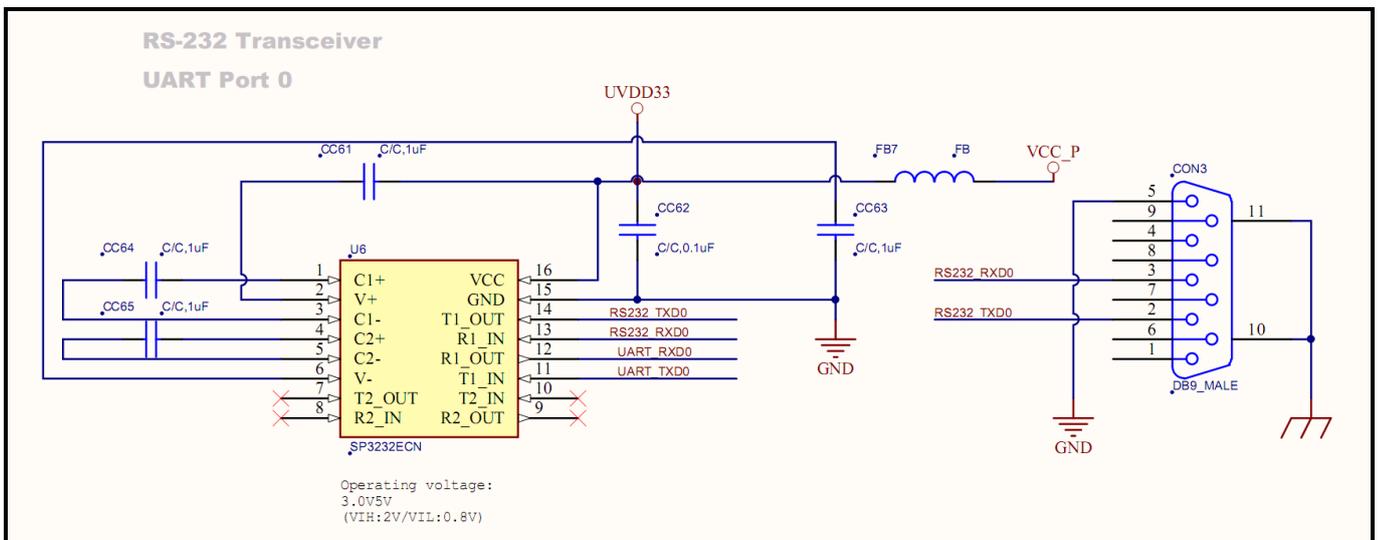
Hình 2.8 Giao tiếp 24LC64

## 2.5 Giao tiếp SPI với bộ nhớ FLASH (W25Q16LC)



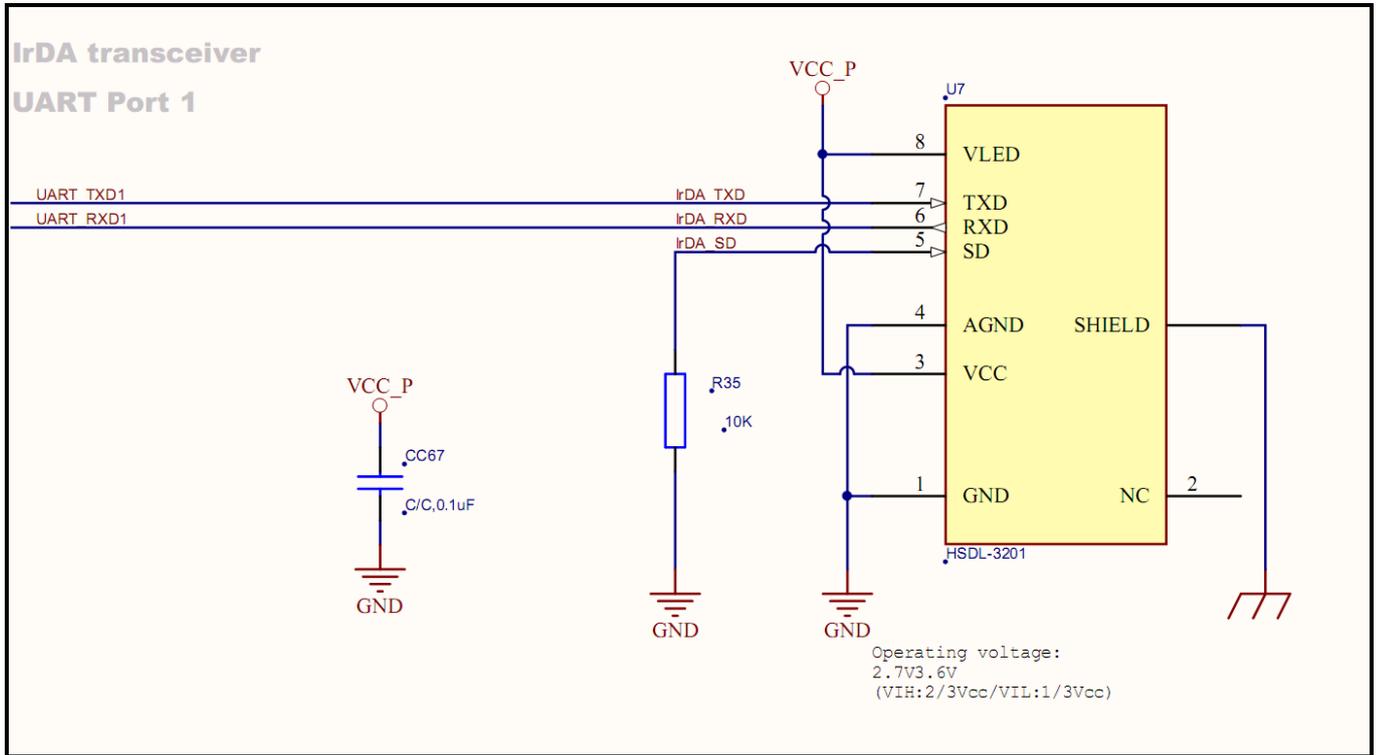
Hình 2.9 Giao tiếp W25Q16LC

## 2.6 Giao tiếp UART



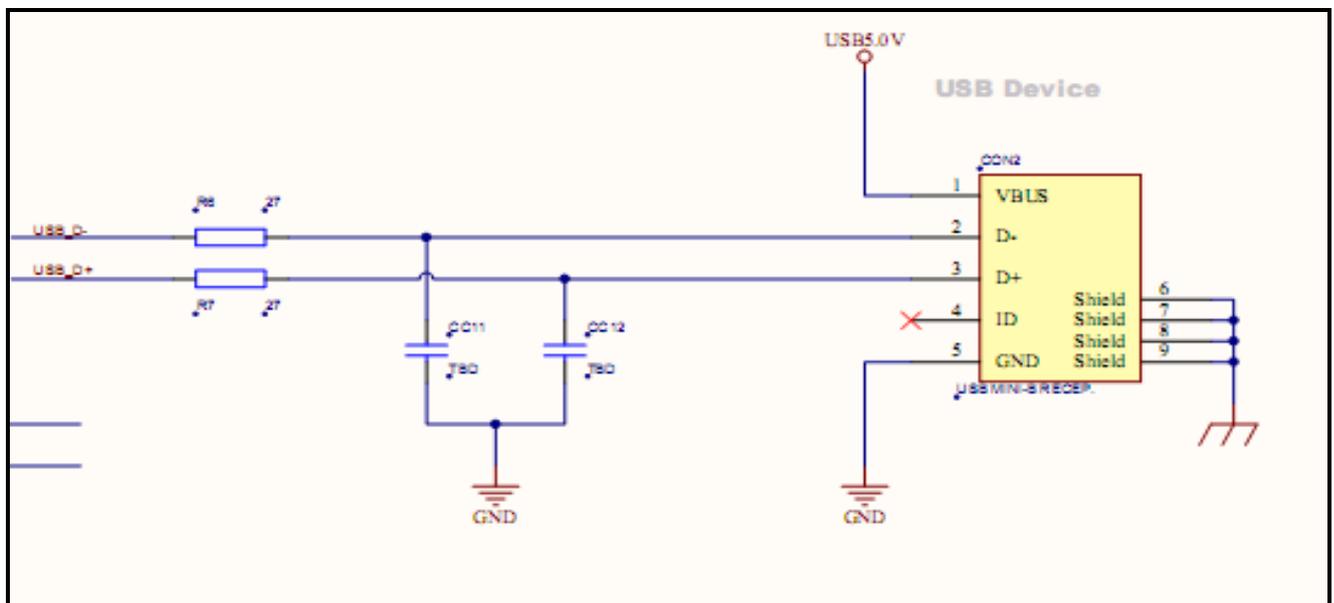
Hình 2.10 Giao tiếp UART

**2.7 Giao tiếp hồng ngoại IrDA (HSDL-3201)**



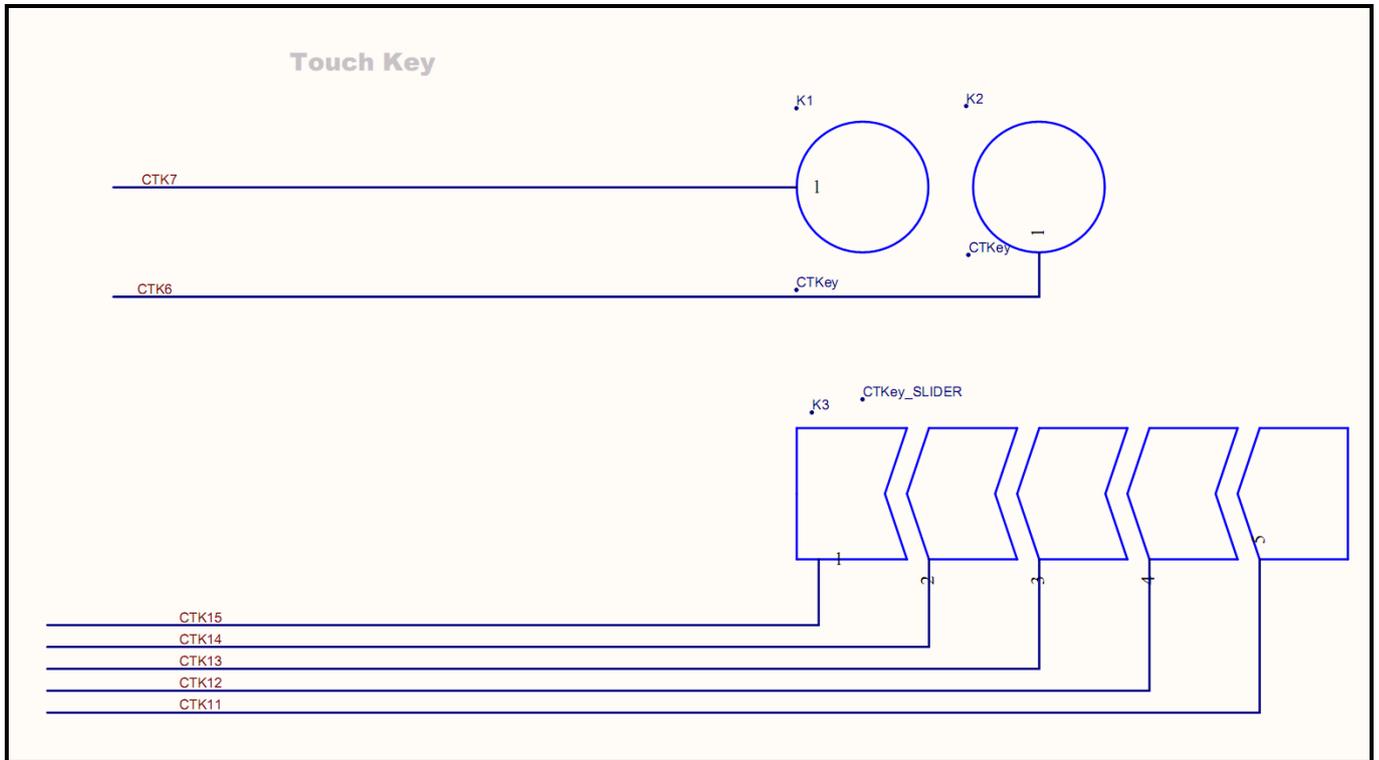
Hình 2.11 Giao tiếp HSDL-3201

**2.8 Giao tiếp USB**



Hình 2.12 Giao tiếp USB

## 2.9 Giao tiếp cảm ứng điện dung (Touch Key)



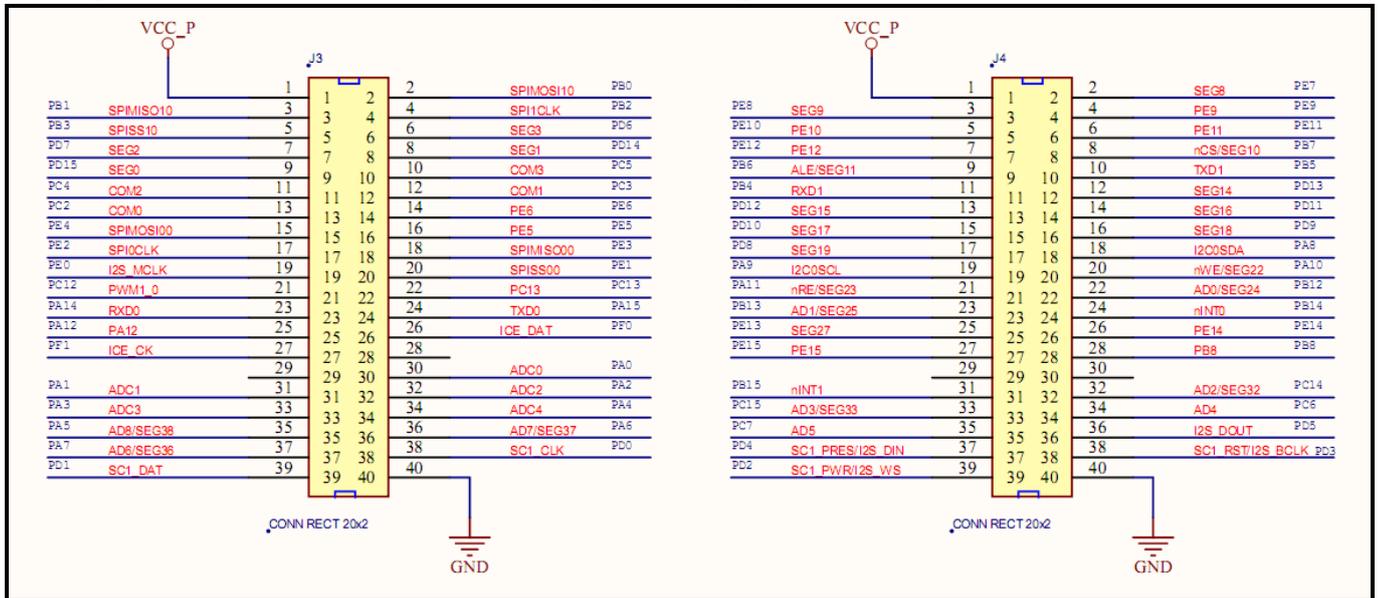
Hình 2.13 Giao tiếp phím cảm ứng



### 3. Chân cắm mở rộng và bảng chức năng các chân I/O

#### 3.1 Chân cắm mở rộng

Hai connector mở rộng J3, J4 nối với các chân tín IO của MCU Nano130KE3BN giúp người sử dụng có thể dễ dàng kết nối, điều khiển các module bên ngoài sử dụng KIT NU-LB-Nano130



Hình 3.1 Connector mở rộng

#### 3.2 Bảng chức năng các chân I/O

Pin No.	Pin Name	Pin Type	Description
1	PE.13	I/O	General purpose digital I/O pin
	LCD_SEG27	O	LCD segment output 27 at LQFP128
2	PB.14	I/O	General purpose digital I/O pin

Pin No.	Pin Name	Pin Type	Description
	INT0	I	External interrupt0 input pin
	SC2_CD	I	SmartCard2 card detect
	SPI2_SS1	O	SPI2 2nd slave select pin
	LCD_SEG12	O	LCD segment output 12 at LQFP64
	LCD_SEG26	O	LCD segment output 26 at LQFP128
3	PB.13	I/O	General purpose digital I/O pin
	EBI_AD1	I/O	EBI Address/Data bus bit1
	LCD_SEG11	O	LCD segment output 11 at LQFP64
	LCD_SEG25	O	LCD segment output 25 at LQFP128
4	PB.12	I/O	General purpose digital I/O pin
	EBI_A0	I/O	EBI Address/Data bus bit0
	CLKO	O	Frequency Divider output pin
	LCD_SEG10	O	LCD segment output 10 at LQFP64
	LCD_SEG24	O	LCD segment output 24 at LQFP128
5			NC
6	X32O	O	External 32.768 kHz crystal output pin
7	X32I	I	External 32.768 kHz crystal input pin
8			NC
9	PA.11	I/O	General purpose digital I/O pin
	I2C1_SCL	I/O	I2C 1 clock pin

Pin No.	Pin Name	Pin Type	Description
	EBI_nRD	O	EBI read enable output pin
	SCO_RST	O	SmartCard0 RST pin
	SPI2_MOSI0	I/O	SPI2 1st MOSI (Master Out, Slave In) pin
	LCD_SEG9	O	LCD segment output 9 at LQFP64
	LCD_SEG23	O	LCD segment output 23 at LQFP128
10	PA.10	I/O	General purpose digital I/O pin
	I2C1_SDA	I/O	I2C 1 data I/O pin
	EBI_nWR	O	EBI write enable output pin
	SCO_PWR	O	SmartCard0 Power pin
	SPI2_MISO0	I/O	SPI2 1st MISO (Master In, Slave Out) pin
	LCD_SEG8	O	LCD segment output 8 at LQFP64
	LCD_SEG22	O	LCD segment output 22 at LQFP128
11	PA.9	I/O	General purpose digital I/O pin
	I2C0_SCL	I/O	I2C 0 clock pin
	SCO_DAT	I/O	SmartCard0 DATA pin
	SPI2_CLK	O	SPI2 serial clock pin
	LCD_SEG7	O	LCD segment output 7 at LQFP64
	LCD_SEG21	O	LCD segment output 21 at LQFP128
12	PA.8	I/O	General purpose digital I/O pin
	I2C0_SDA	I/O	I2C 0 data I/O pin

Pin No.	Pin Name	Pin Type	Description
	SCO_CLK	O	SmartCard0 clock pin
	SPI2_SSO	O	SPI2 1st slave select pin
	LCD_SEG6	O	LCD segment output 6 at LQFP64
	LCD_SEG20	O	LCD segment output 20 at LQFP128
13	PD.8	I/O	General purpose digital I/O pin
	LCD_SEG19	O	LCD segment output 19 at LQFP128
14	PD.9	I/O	General purpose digital I/O pin
	LCD_SEG18	O	LCD segment output 18 at LQFP128
15	PD.10	I/O	General purpose digital I/O pin
	LCD_SEG17	O	LCD segment output 17 at LQFP128
16	PD.11	I/O	General purpose digital I/O pin
	LCD_SEG16	O	LCD segment output 16 at LQFP128
17	PD.12	I/O	General purpose digital I/O pin
	LCD_SEG15	O	LCD segment output 15 at LQFP128
18	PD.13	I/O	General purpose digital I/O pin
	LCD_SEG14	O	LCD segment output 14 at LQFP128
19	PB.4	I/O	General purpose digital I/O pin
	UART1_RXD	I	UART1 Data receiver input pin
	SCO_CD	I	SmartCard0 card detect pin
	SPI2_SSO	O	SPI2 1st slave select pin

Pin No.	Pin Name	Pin Type	Description
	LCD_SEG5	O	LCD segment output 5 at LQFP64
	LCD_SEG13	O	LCD segment output 13 at LQFP128
20	PB.5	I/O	General purpose digital I/O pin
	UART1_TXD	O	UART1 Data transmitter output pin
	SC0_RST	O	SmartCard0 RST pin
	SPI2_CLK	O	SPI2 serial clock pin
	LCD_SEG4	O	LCD segment output 4 at LQFP64
	LCD_SEG12	O	LCD segment output 12 at LQFP128
21	PB.6	I/O	General purpose digital I/O pin
	UART1_nRTS	O	UART1 Request to Send output pin
	EBI_ALE	O	EBI address latch enable output pin
	SPI2_MISO0	I/O	SPI2 2nd MISO (Master In, Slave Out) pin
	LCD_SEG3	O	LCD segment output 3 at LQFP64
	LCD_SEG11	O	LCD segment output 11 at LQFP128
22	PB.7	I/O	General purpose digital I/O pin
	UART1_nCTS	I	UART1 Clear to Send input pin
	EBI_nCS	O	EBI chip select enable output pin
	SPI2_MOSI0	I/O	SPI2 1st MOSI (Master Out, Slave In) pin
	LCD_SEG2	O	LCD segment output 2 at LQFP64
	LCD_SEG10	O	LCD segment output 10 at LQFP128

Pin No.	Pin Name	Pin Type	Description
23			NC
24	LDO_CAP	P	LDO output pin
25			NC
26			NC
27	VDD	P	Power supply for I/O ports and LDO source
28			NC
29	VSS	P	Ground
30	VSS	P	Ground
31	VSS	P	Ground
32	VSS	P	Ground
33	PE.12	I/O	General purpose digital I/O pin
34	PE.11	I/O	General purpose digital I/O pin
35	PE.10	I/O	General purpose digital I/O pin
36	PE.9	I/O	General purpose digital I/O pin
37	PE.8	I/O	General purpose digital I/O pin
	LCD_SEG9	O	LCD segment output 9 at LQFP128
38	PE.7	I/O	General purpose digital I/O pin
	LCD_SEG8	O	LCD segment output 8 at LQFP128
39			NC
40	USB_VBUS	USB	POWER SUPPLY: From USB Host or HUB.

Pin No.	Pin Name	Pin Type	Description
41	USB_VDD33_C AP	USB	Internal Power Regulator Output 3.3V Decoupling Pin
42	USB_D-	USB	USB Differential Signal D-
43	USB_D+	USB	USB Differential Signal D+
44	PB.0	I/O	General purpose digital I/O pin
	UART0_RXD	I	UART0 Data receiver input pin
	SPI1_MOSIO	I/O	SPI1 1st MOSI (Master Out, Slave In) pin
	LCD_SEG1	O	LCD segment output 1 at LQFP64
	LCD_SEG7	O	LCD segment output 7 at LQFP128
45	PB.1	I/O	General purpose digital I/O pin
	UART0_TXD	O	UART0 Data transmitter output pin
	SPI1_MISO0	I/O	SPI1 1st MISO (Master In, Slave Out) pin
	LCD_SEG0	O	LCD segment output 0 at LQFP64
	LCD_SEG6	O	LCD segment output 6 at LQFP128
46	PB.2	I/O	General purpose digital I/O pin
	UART0_nRTS	O	UART0 Request to Send output pin
	EBI_nWRL	O	EBI low byte write enable output pin
	SPI1_CLK	O	SPI1 serial clock pin
	LCD_COM3	O	LCD common output 3 at LQFP64
	LCD_SEG5	O	LCD segment output 5 at LQFP128
47	PB.3	I/O	General purpose digital I/O pin

Pin No.	Pin Name	Pin Type	Description
	UART0_nCTS	I	UART0 Clear to Send input pin
	EBI_nWRH	O	EBI high byte write enable output pin
	SPI1_SS0	O	SPI1 1st slave select pin
	LCD_COM2	O	LCD common output 2 at LQFP64
	LCD_SEG4	O	LCD segment output 4 at LQFP128
48	PD.6	I/O	General purpose digital I/O pin
	LCD_SEG3	O	LCD segment output 3 at LQFP128
49	PD.7	I/O	General purpose digital I/O pin
	LCD_SEG2	O	LCD segment output 2 at LQFP128
50	PD.14	I/O	General purpose digital I/O pin
	LCD_SEG1	O	LCD segment output 1 at LQFP128
51	PD.15	I/O	General purpose digital I/O pin
	LCD_SEG0	O	LCD segment output 0 at LQFP128
52	PC.5	I/O	General purpose digital I/O pin
	SPIO_MOSI1	O	SPIO 2nd MOSI (Master Out, Slave In) pin
	LCD_COM3	O	LCD common output 3 at LQFP128
53	PC.4	I/O	General purpose digital I/O pin
	SPIO_MISO1	I	SPIO 2nd MISO (Master In, Slave Out) pin
	LCD_COM2	O	LCD common output 2 at LQFP128
54	PC.3	I/O	General purpose digital I/O pin

Pin No.	Pin Name	Pin Type	Description
	SPI0_MOSIO	O	SPI0 1st MOSI (Master Out, Slave In) pin
	I2S_DO	O	I2S data output
	SC1_RST	O	SmartCard1 RST pin
	LCD_COM1	O	LCD common output 1 at LQFP64
	LCD_COM1	O	LCD common output 1 at LQFP128
55	PC.2	I/O	General purpose digital I/O pin
	SPI0_MISO0	I	SPI0 1st MISO (Master In, Slave Out) pin
	I2S_DI	I	I2S data input
	SC1_PWR	O	SmartCard1 PWR pin
	LCD_COM0	O	LCD common output 0 at LQFP64
	LCD_COM0	O	LCD common output 0 at LQFP128
56	PC.1	I/O	General purpose digital I/O pin
	SPI0_CLK	I/O	SPI0 serial clock pin
	I2S_BCLK	I/O	I2S bit clock pin
	SC1_DAT	I/O	SmartCard1 DATA pin
	LCD_DH2	O	LCD external capacitor pin of charge pump circuit at LQFP64
	LCD_DH2	O	LCD external capacitor pin of charge pump circuit at LQFP128
57	PC.0	I/O	General purpose digital I/O pin
	SPI0_SS0	I/O	SPI0 1st slave select pin

Pin No.	Pin Name	Pin Type	Description
	I2S_LRCLK	I/O	I2S left right channel clock
	SC1_CLK	O	SmartCard1 clock pin
	LCD_DH1	O	LCD external capacitor pin of charge pump circuit at LQFP64
	LCD_DH1	O	LCD external capacitor pin of charge pump circuit at LQFP128
58	PE.6	I/O	General purpose digital I/O pin
59	LCD_VLCD	AO	LCD power supply pin
60			NC
61	PE.5		General purpose digital I/O pin
62	PB.11	I/O	General purpose digital I/O pin
	PWM1_CH0	I/O	PWM1 Channel0 output
	TM3	O	Timer3 external counter input
	SC2_DAT	I/O	SmartCard2 DATA pin
	SPI0_MISO0	I/O	SPI0 1st MISO (Master In, Slave Out) pin
	LCD_V1	O	LCD Unit voltage for LCD charge pump circuit at LQFP64
	LCD_V1	O	LCD Unit voltage for LCD charge pump circuit at LQFP128
63	PB.10	I/O	General purpose digital I/O pin
	SPI0_SS1	I/O	SPI0 2nd slave select pin
	TM2	O	Timer2 external counter input

Pin No.	Pin Name	Pin Type	Description
	SC2_CLK	O	SmartCard2 clock pin
	SPI0_MOSI0	I/O	SPI0 1st MOSI (Master Out, Slave In) pin
	LCD_V2	O	LCD driver biasing voltage at LQFP64
	LCD_V2	O	LCD driver biasing voltage at LQFP128
64	PB.9	I/O	General purpose digital I/O pin
	SPI1_SS1	I/O	SPI1 2nd slave select pin
	TM1	O	Timer1 external counter input
	SC2_RST	O	SmartCard2 RST pin
	INT0	I	External interrupt0 input pin
	LCD_V3	O	LCD driver biasing voltage at LQFP64
	LCD_V3	O	LCD driver biasing voltage at LQFP128
65	PE.4	I/O	General purpose digital I/O pin
	SPI0_MOSI0	I/O	SPI0 1st MOSI (Master Out, Slave In) pin
66	PE.3	I/O	General purpose digital I/O pin
	SPI0_MISO0	I/O	SPI0 1st MISO (Master In, Slave Out) pin
67	PE.2	I/O	General purpose digital I/O pin
	SPI0_CLK	O	SPI0 serial clock pin
68	PE.1	I/O	General purpose digital I/O pin
	PWM1_CH3	I/O	PWM1 Channel3 output
	SPI0_SSO	O	SPI0 1st slave select pin

Pin No.	Pin Name	Pin Type	Description
69	PE.0	I/O	General purpose digital I/O pin
	PWM1_CH2	I/O	PWM1 Channel2 output
	I2S_MCLK	O	I2S master clock output pin
70	PC.13	I/O	General purpose digital I/O pin
	SPI1_MOSI1	O	SPI1 2nd MOSI (Master Out, Slave In) pin
	PWM1_CH1	O	PWM1 Channel1 output
	SNOOPER	I	Snooper pin
	INT0	I	External interrupt 0 input pin
	I2C0_SCL	O	I2C 0 clock pin
71	PC.12	I/O	General purpose digital I/O pin
	SPI1_MISO1	I	SPI1 2nd MISO (Master In, Slave Out) pin
	PWM1_CH0	O	PWM1 Channel0 output
	INT0	I	External interrupt0 input pin
	I2C0_SDA	I/O	I2C 0 data I/O pin
72	PC.11	I/O	General purpose digital I/O pin
	SPI1_MOSI0	O	SPI1 1st MOSI (Master Out, Slave In) pin
	UART1_TXD	O	UART1 Data transmitter output pin
	CTK15	I	Touch key 15
	LCD_SEG31	O	LCD segment output 31 at LQFP64
73	PC.10	I/O	General purpose digital I/O pin

Pin No.	Pin Name	Pin Type	Description
	SPI1_MISO0	I	SPI1 1st MISO (Master In, Slave Out) pin
	UART1_RXD	I	UART1 Data receiver input pin
	CTK14	I	Touch key 14
	LCD_SEG30	O	LCD segment output 30 at LQFP64
74	PC.9	I/O	General purpose digital I/O pin
	SPI1_CLK	I/O	SPI1 serial clock pin
	I2C1_SCL	I/O	I2C 1 clock pin
	CTK13	I	Touch key 13
	LCD_SEG29	O	LCD segment output 29 at LQFP64
75	PC.8	I/O	General purpose digital I/O pin
	SPI1_SS0	I/O	SPI1 1st slave select pin
	EBI_MCLK	O	EBI external clock output pin
	I2C1_SDA	I/O	I2C 1 data I/O pin
	CTK12	I	Touch key 12
	LCD_SEG28	O	LCD segment output 28 at LQFP64
76	PA.15	I/O	General purpose digital I/O pin
	PWM0_CH3	I/O	PWM0 Channel3 output
	I2S_MCLK	O	I2S master clock output pin
	TC3	I	Timer3 capture input
	SCO_PWR	O	SmartCard0 Power pin

Pin No.	Pin Name	Pin Type	Description
	UART0_TXD	O	UART0 Data transmitter output pin
	LCD_SEG27	O	LCD segment output 27 at LQFP64
77	PA.14	I/O	General purpose digital I/O pin
	PWM0_CH2	I/O	PWM0 Channel2 output
	EBI_AD15	I/O	EBI Address/Data bus bit15
	TC2	I	Timer 2 capture input
	UART0_RXD	I	UART0 Data receiver input pin
	LCD_SEG26	O	LCD segment output 26 at LQFP64
78	PA.13	I/O	General purpose digital I/O pin
	PWM0_CH1	I/O	PWM0 Channel1 output
	EBI_AD14	I/O	EBI Address/Data bus bit14
	TC1	I	Timer1 capture input
	I2C0_SCL	I/O	I2C 0 clock pin
	CTK11	I	Touch key 11
	LCD_SEG25	O	LCD segment output 25 at LQFP64
79	PA.12	I/O	General purpose digital I/O pin
	PWM0_CH0	I/O	PWM0 Channel0 output
	EBI_AD13	I/O	EBI Address/Data bus bit13
	TC0	I	Timer 0 capture input
	I2C0_SDA	I/O	I2C 0 data I/O pin

Pin No.	Pin Name	Pin Type	Description
	CTK10	I	Touch key 10
	LCD_SEG24	O	LCD segment output 24 at LQFP64
80	ICE_DAT	I/O	Serial Wired Debugger Data pin
	PF.0	I/O	General purpose digital I/O pin
	INT0	I	External interrupt0 input pin
81	ICE_CLK	I	Serial Wired Debugger Clock pin
	PF.1	I/O	General purpose digital I/O pin
	CLKO	O	Frequency Divider output pin
	INT1	I	External interrupt1 input pin
82			NC
83	VDD	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit
84			NC
85	VSS	P	Ground
86	VSS	P	Ground
87	AVSS	AP	Ground Pin for analog circuit
88	AVSS	AP	Ground Pin for analog circuit
89	PA.0	I/O	General purpose digital I/O pin
	AD0	AI	ADC analog input0
	SC2_CD	I	SmartCard2 card detect
	CTK8	AI	Touch key 1

Pin No.	Pin Name	Pin Type	Description
90	PA.1	I/O	General purpose digital I/O pin
	AD1	AI	ADC analog input1
	EBI_AD12	I/O	EBI Address/Data bus bit12
	CTK9	AI	Touch key 9
91	PA.2	I/O	General purpose digital I/O pin
	AD2	AI	ADC analog input2
	EBI_AD11	I/O	EBI Address/Data bus bit11
	UART1_RXD	I	UART1 Data receiver input pin
	LCD_SEG23	AO	LCD segment output 23 at LQFP64
92	PA.3	I/O	General purpose digital I/O pin
	AD3	AI	ADC analog input3
	EBI_AD10	I/O	EBI Address/Data bus bit10
	UART1_TXD	O	UART1 Data transmitter output pin
	LCD_SEG22	AO	LCD segment output 22 at LQFP64
93	PA.4	I/O	General purpose digital I/O pin
	AD4	AI	ADC analog input4
	EBI_AD9	I/O	EBI Address/Data bus bit9
	SC2_PWR	O	SmartCard2 Power pin
	I2C0_SDA	I/O	I2C 0 data I/O pin
	LCD_SEG21	AO	LCD segment output 21 at LQFP64

Pin No.	Pin Name	Pin Type	Description
	LCD_SEG39	AO	LCD segment output 39 at LQFP128
94	PA.5	I/O	General purpose digital I/O pin
	AD5	AI	ADC analog input5
	EBI_AD8	I/O	EBI Address/Data bus bit8
	SC2_RST	O	SmartCard2 RST pin
	I2C0_SCL	I/O	I2C 0 clock pin
	LCD_SEG20	AO	LCD segment output 20 at LQFP64
	LCD_SEG38	AO	LCD segment output 38 at LQFP128
95	PA.6	I/O	General purpose digital I/O pin
	AD6	AI	ADC analog input6
	EBI_AD7	I/O	EBI Address/Data bus bit7
	TC3	I	Timer3 capture input
	SC2_CLK	O	SmartCard2 clock pin
	PWM0_CH3	O	PWM0 Channel3 output
	LCD_SEG19	AO	LCD segment output 19 at LQFP64
	LCD_SEG37	AO	LCD segment output 37 at LQFP128
96	PA.7	I/O	General purpose digital I/O pin
	AD7	AI	ADC analog input7
	EBI_AD6	I/O	EBI Address/Data bus bit6
	TC2	I	Timer2 capture input

Pin No.	Pin Name	Pin Type	Description
	SC2_DAT	I/O	SmartCard2 DATA pin
	PWM0_CH2	O	PWM0 Channel2 output
	CTK_CAP	AI	Touch key Capacitor pin
	LCD_SEG18	AO	LCD segment output 18 output at LQFP64
	LCD_SEG36	AO	LCD segment output 36 output at LQFP128
97	VREF	AP	Voltage reference input for ADC
98			NC
99	AVDD	AP	Power supply for internal analog circuit
100	PD.0	I/O	General purpose digital I/O pin
	UART1_RXD	I	UART1 Data receiver input pin
	SPI2_SS0	I/O	SPI2 2nd slave select pin
	SC1_CLK	O	SmartCard1 clock pin
	CTK0	AI	Touch key 0
	AD8	AI	ADC analog input8
101	PD.1	I/O	General purpose digital I/O pin
	TX1	O	UART1 Data transmitter output pin
	SPI2_CLK	I/O	SPI2 serial clock pin
	SC1_DAT	I/O	SmartCard1 DATA pin
	AD9	AI	ADC analog input9
	CTK1	AI	Touch key 1

Pin No.	Pin Name	Pin Type	Description
102	PD.2	I/O	General purpose digital I/O pin
	UART1_nRTS		UART1 Request to Send output pin
	I2S_LRCLK	I/O	I2S left right channel clock
	SPI2_MISO0	I	SPI2 1st MISO (Master In, Slave Out) pin
	SC1_PWR	O	SmartCard1 Power pin
	AD10	AI	ADC analog input10
	CTK2	AI	Touch key 2
103	PD.3	I/O	General purpose digital I/O pin
	UART1_nCTS		UART1 Clear to Send input pin
	I2S_BCLK	I/O	I2S bit clock pin
	SPI2_MOSI0	O	SPI2 1st MOSI (Master Out, Slave In) pin
	SC1_RST	O	SmartCard1 RST pin
	AD11	AI	ADC analog input11
	CTK3	AI	Touch key 3
104			NC
105	PD.4	I/O	General purpose digital I/O pin
	I2S_DI	I	I2S data input
	SPI2_MISO1	I	SPI2 2nd MISO (Master In, Slave Out) pin
	SC1_CD	I	SmartCard1 card detect
	CTK4	AI	Touch key 4

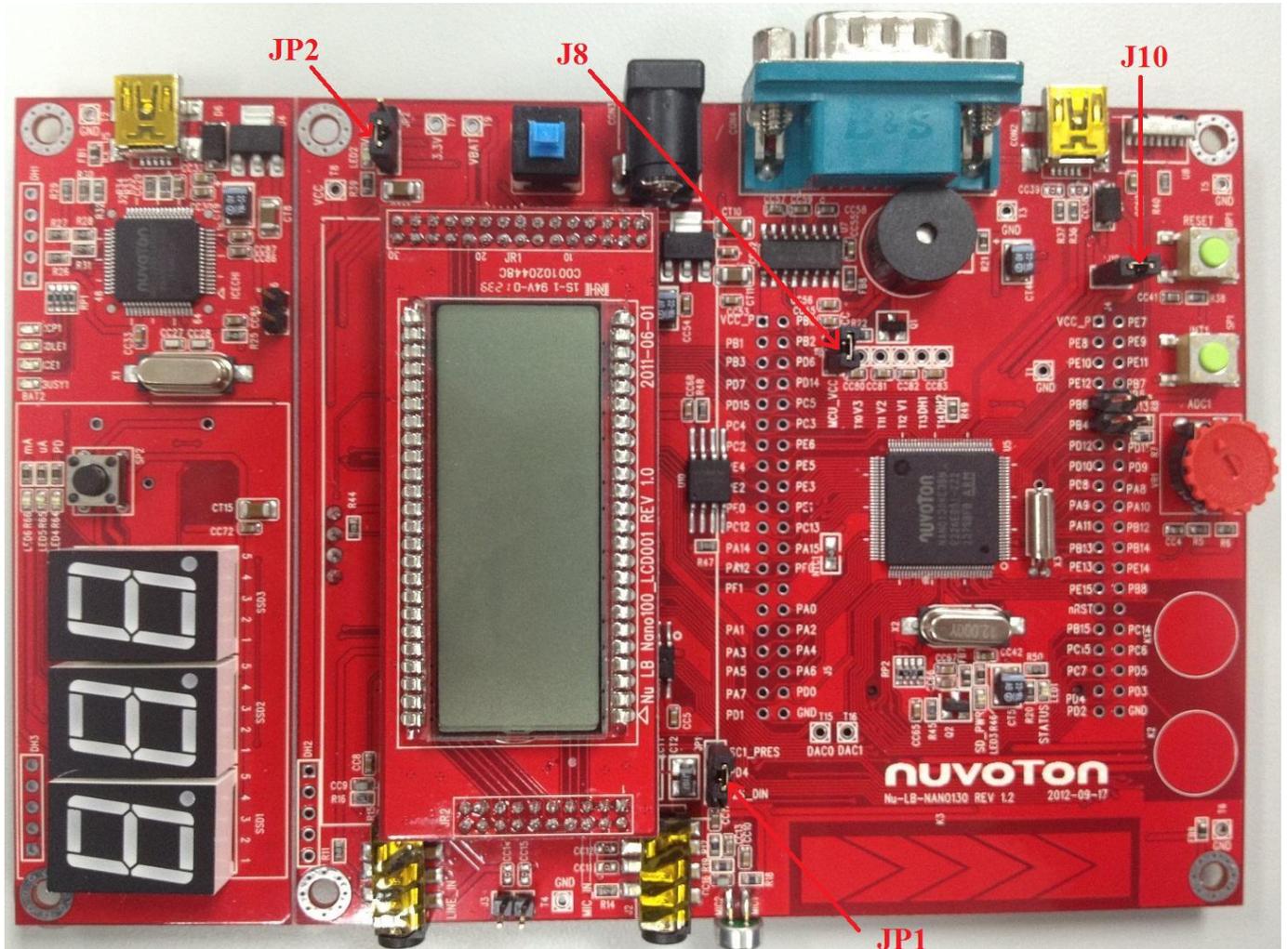
Pin No.	Pin Name	Pin Type	Description
	LCD_SEG35	AO	LCD segment output 35 at LQFP128
106	PD.5	I/O	General purpose digital I/O pin
	I2S_DO	O	I2S data output
	SPI2_MOSI1	O	SPI2 2nd MOSI (Master Out, Slave In) pin
	CTK5	AI	Touch key 5
	LCD_SEG34	AO	LCD segment output 34 at LQFP128
107	PC.7	I/O	General purpose digital I/O pin
	DA1_OUT	AO	DAC 1 output
	EBI_AD5	I/O	EBI Address/Data bus bit5
	TC1	I	Timer1 capture input
	PWM0_CH1	O	PWM1 Channel1 output
	LCD_SEG17	AO	LCD segment output 17 at LQFP64
108	PC.6	I/O	General purpose digital I/O pin
	DA0_OUT	I	DAC0 output
	EBI_AD4	I/O	EBI Address/Data bus bit4
	TC0	I	Timer 0 capture input
	SC1_CD		SmartCard1 card detect pin
	PWM0_CH0	O	PWM0 Channel0 output
109	PC.15	I/O	General purpose digital I/O pin
	EBI_AD3	I/O	EBI Address/Data bus bit3

Pin No.	Pin Name	Pin Type	Description
	TC0	I	Timer0 capture input
	PWM1_CH2	O	PWM1 Channel1 output
	LCD_SEG16	AO	LCD segment output 16 at LQFP64
	LCD_SEG33	AO	LCD segment output 33 at LQFP128
110	PC.14	I/O	General purpose digital I/O pin
	EBI_AD2	I/O	EBI Address/Data bus bit2
	PWM1_CH3	I/O	PWM1 Channel3 output
	LCD_SEG15	AO	LCD segment output 15 at LQFP64
	LCD_SEG32	AO	LCD segment output 32 at LQFP128
111	PB.15	I/O	General purpose digital I/O pin
	INT1	I	External interrupt1 input pin
	SNOOPER	I	Snooper pin
	SC1_CD	I	SmartCard1 card detect
	LCD_SEG14	AO	LCD segment output 14 at LQFP64
	LCD_SEG31	AO	LCD segment output 31 at LQFP128
112			NC
113	XT1_IN	O	External 4~24 MHz crystal output pin
114	XT1_OUT	I	External 4~24 MHz crystal input pin
115			NC

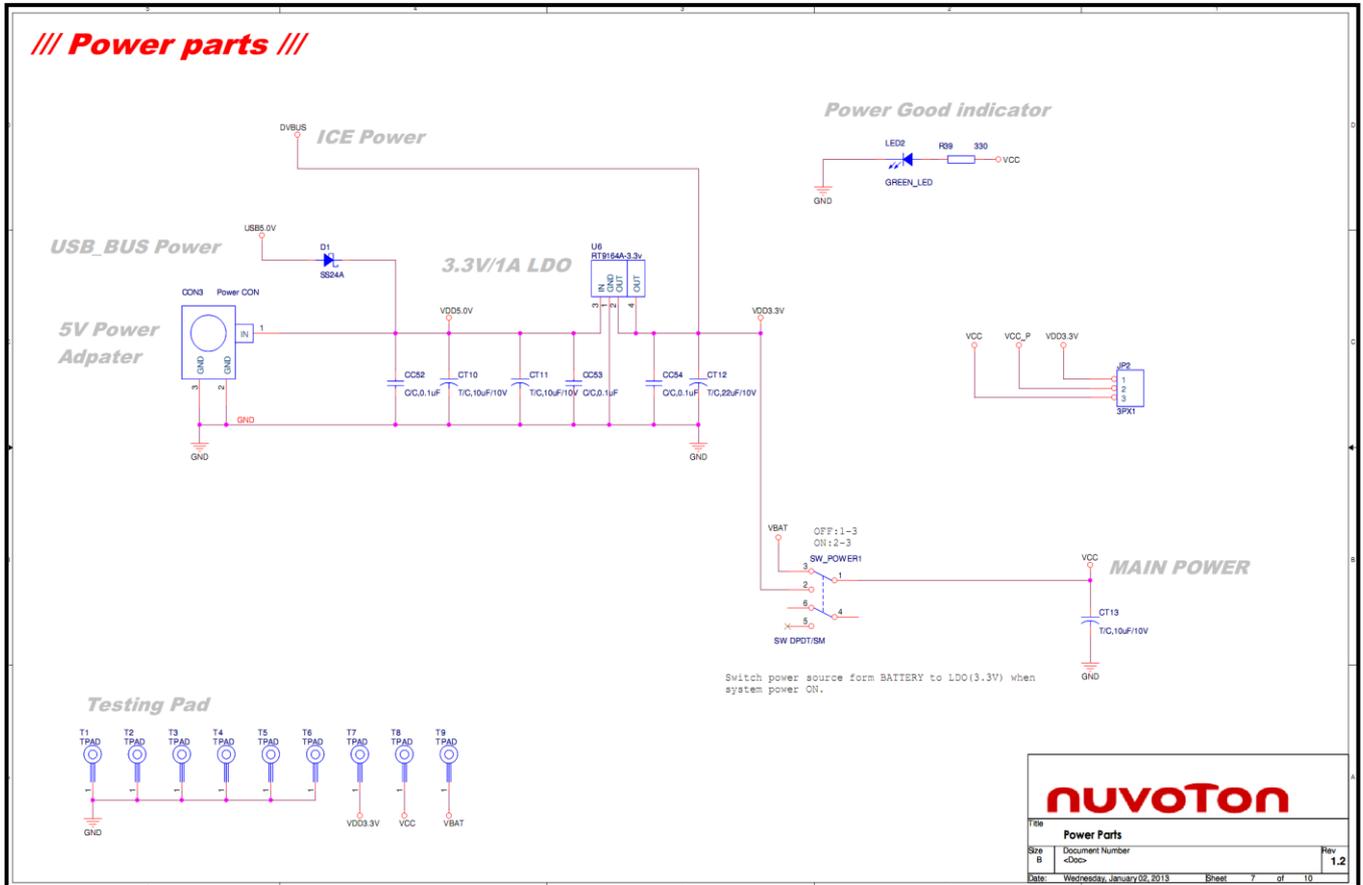
Pin No.	Pin Name	Pin Type	Description
116	nRESET	I	External reset input: Low active, set this pin low reset chip to initial state. With internal pull-up.
117	VSS	P	Ground
118	VSS	P	Ground
119			NC
120	VDD	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit
121			NC
122	PF.4	I/O	General purpose digital I/O pin
	I2C0_SDA	I/O	I2C 0 data I/O pin
	CTK6	AI	Touch key 6
123	PF.5	I/O	Digital GPI/O pin
	I2C0_SCL	I/O	I2C 0 clock pin
	CTK7	AI	Touch key 7
124	VSS	P	Ground
125	PVSS	I/O	PLL Ground
126	PB.8	I/O	General purpose digital I/O pin
	STADC	I	ADC external trigger input.
	TMO	I	Timer0 external counter input
	INT0	I	External interrupt0 input pin
	SC2_PWR	O	SmartCard2 Power pin

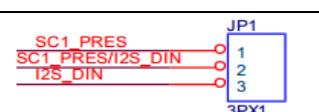
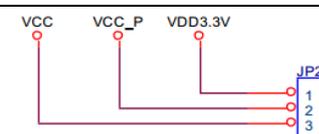
Pin No.	Pin Name	Pin Type	Description
	LCD_SEG13	AO	LCD segment output 13 at LQFP64
	LCD_SEG30	AO	LCD segment output 30 at LQFP128
127	PE.15	I/O	General purpose digital I/O pin
	LCD_SEG29	O	LCD segment output 29 at LQFP128
128	PE.14	I/O	General purpose digital I/O pin
	LCD_SEG28	O	LCD segment output 28 at LQFP128

#### 4. Nguồn và các Jăm nối

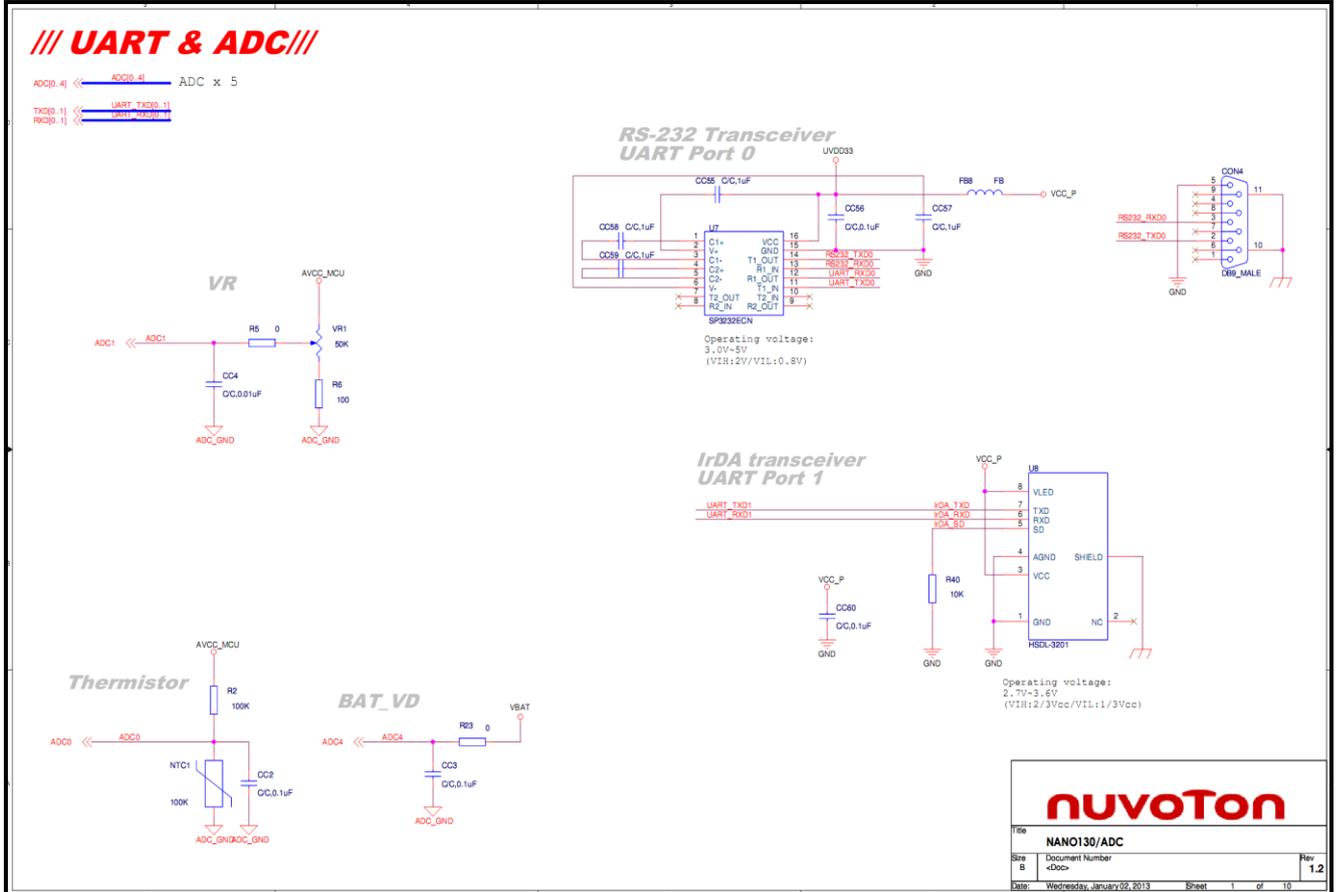


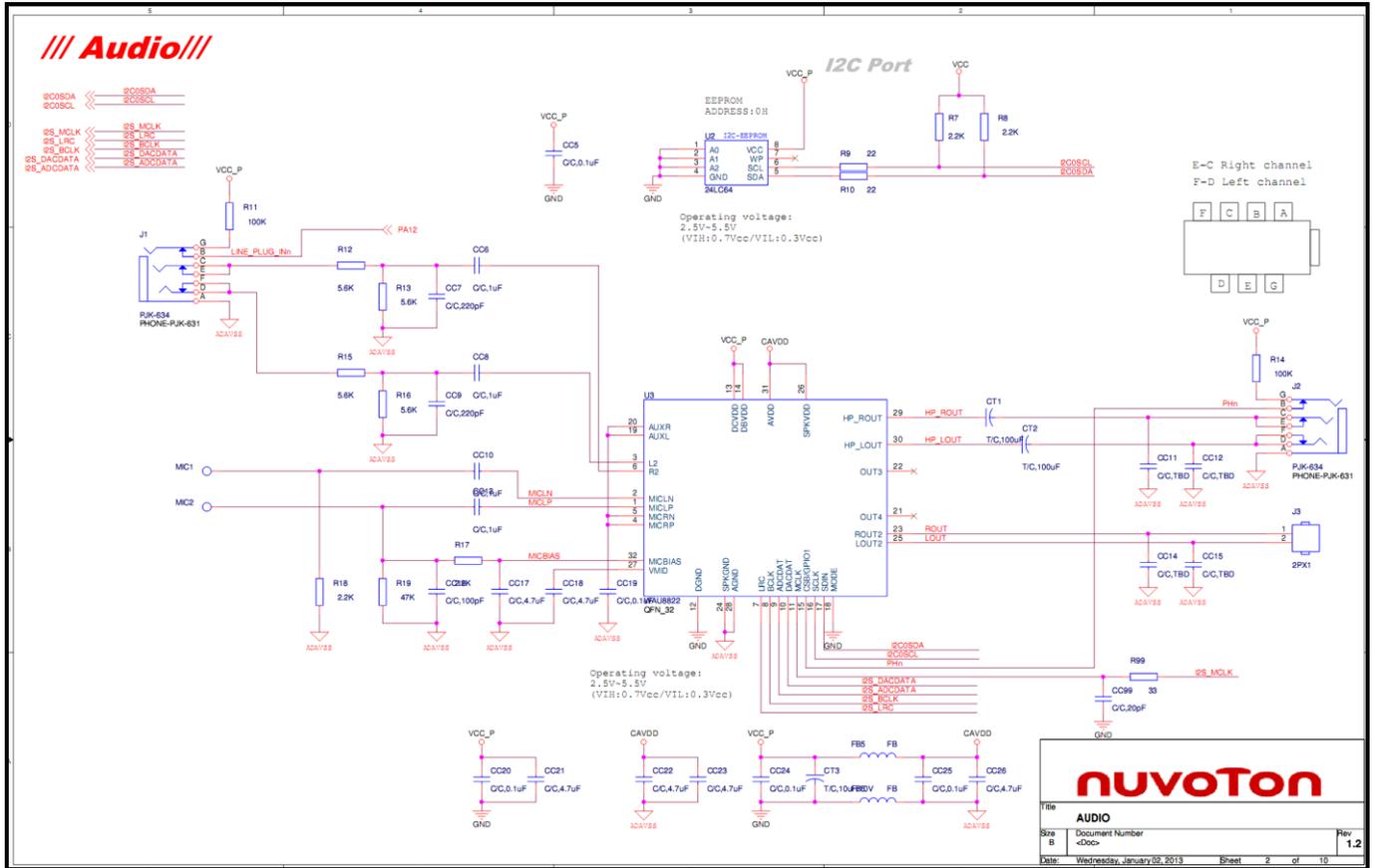
Nguồn	Ghi chú
VDD3.3V	Nguồn ra 3V3 với nguồn vào có thể lấy từ USB, Jac CON3 hoặc VDBUS(từ mạch nạp)
VBAT	Nguồn lấy từ chân T9
VCC	Lấy từ VDD3.3V hoặc VBAT qua công tắc chọn SWDPDT/SM
VCC_P	Nguồn cấp cho các khối SPI flash W25Q16CL, MMC/SD Card, Smart card, RS232, hồng ngoại HSDL-3201, Audio, EEPROM, LCD
VCC_MCU	Nguồn VDD vi điều khiển Nano130KE3BN
AVCC_MCU	Nguồn AVDD vi điều khiển Nano130KE3BN

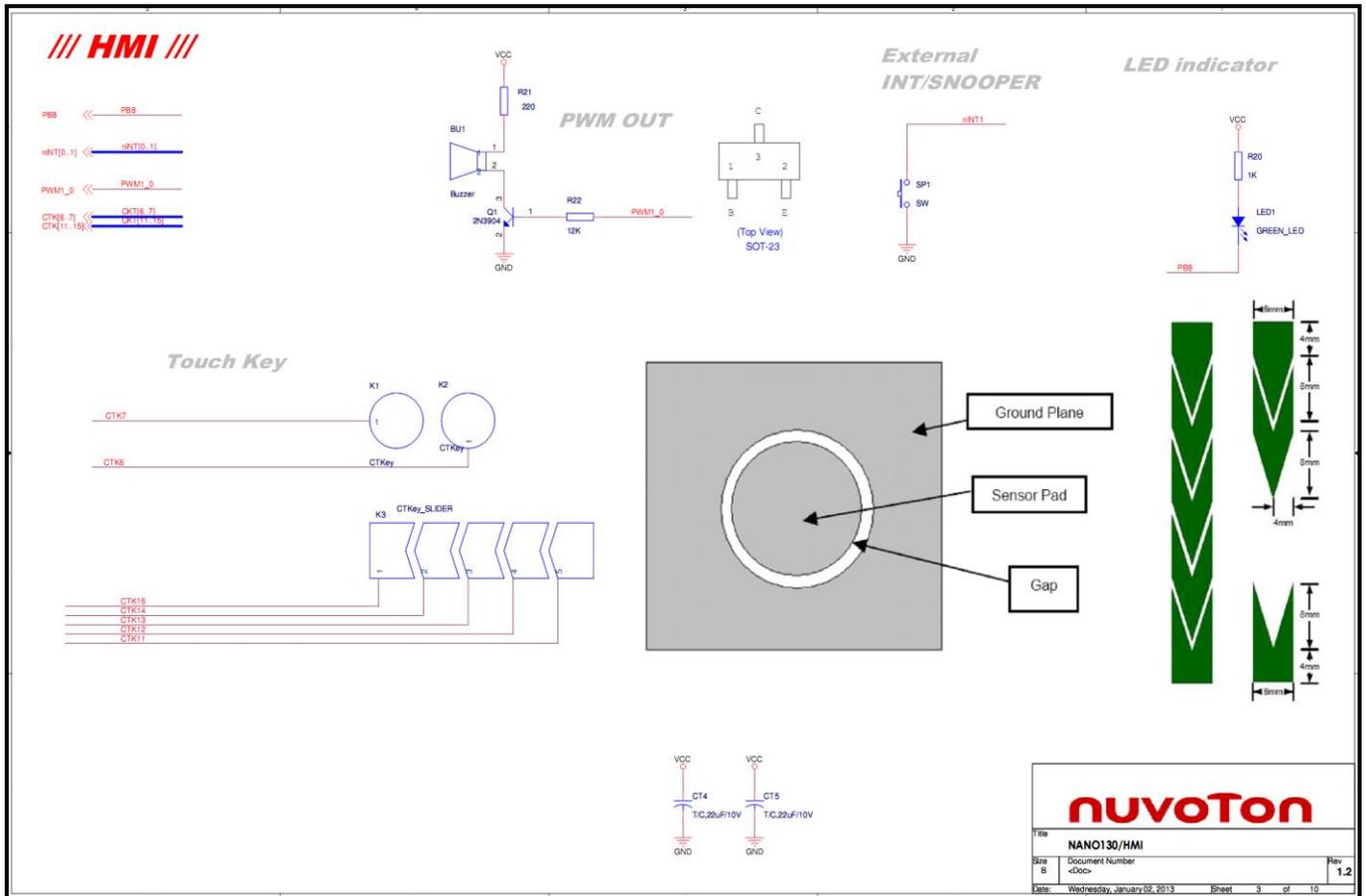


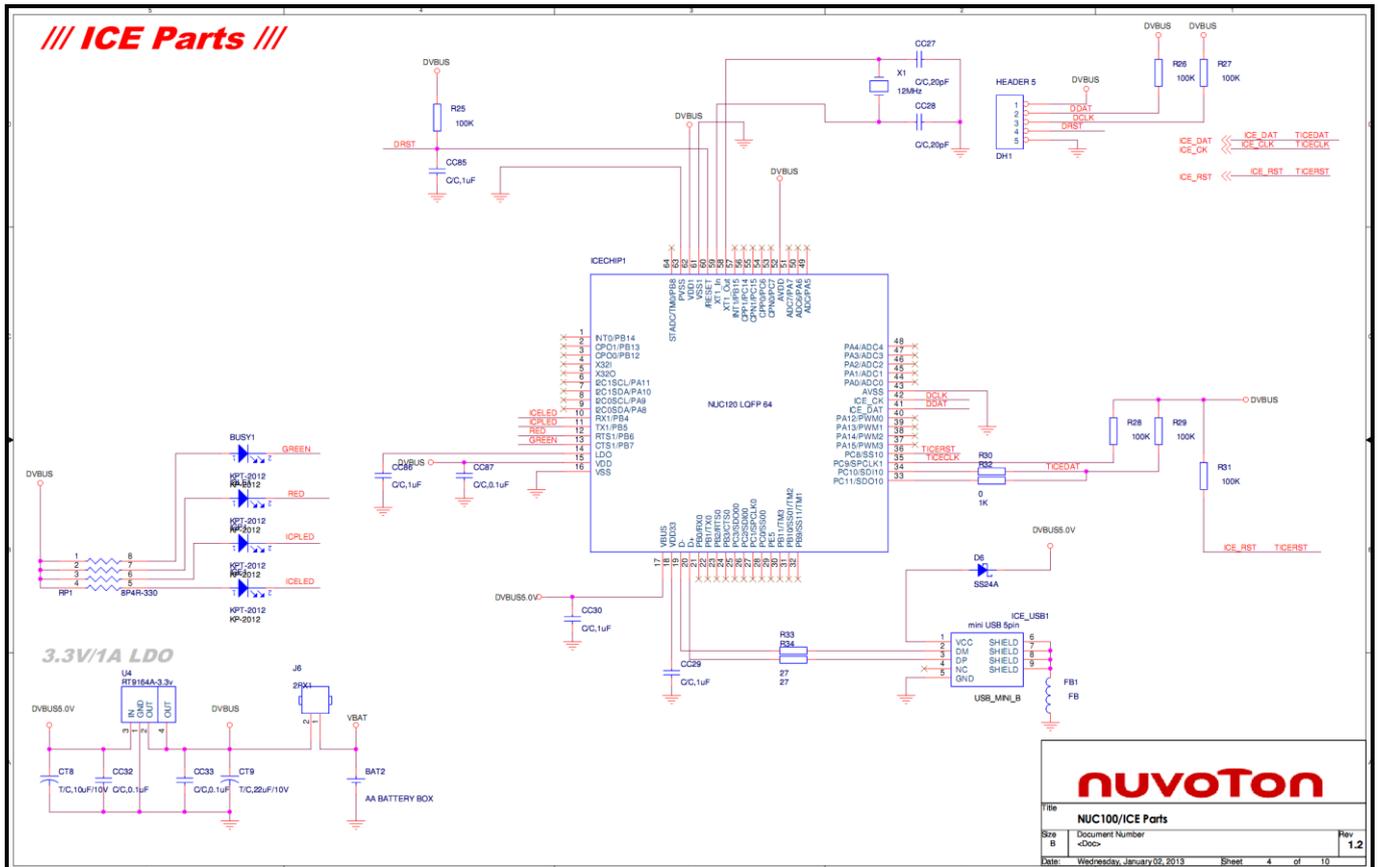
Jam		Ghi chú
JP1		Lựa chọn chức năng chân PD4 1-2: giao tiếp Smart Card 2-3: giao tiếp Audio
JP2		Lựa chọn nguồn vào VPP 1-2: VCC_P lấy từ VDD3.3V 2-3: VCC_P lấy từ VCC
J3		Jac nối với Speaker output of WAU8822
J8		Nối MCU_VCC với VCC
J10		Nối chân Reset của mạch nạp với chân Reset của vi điều khiển Nano130KE3BN

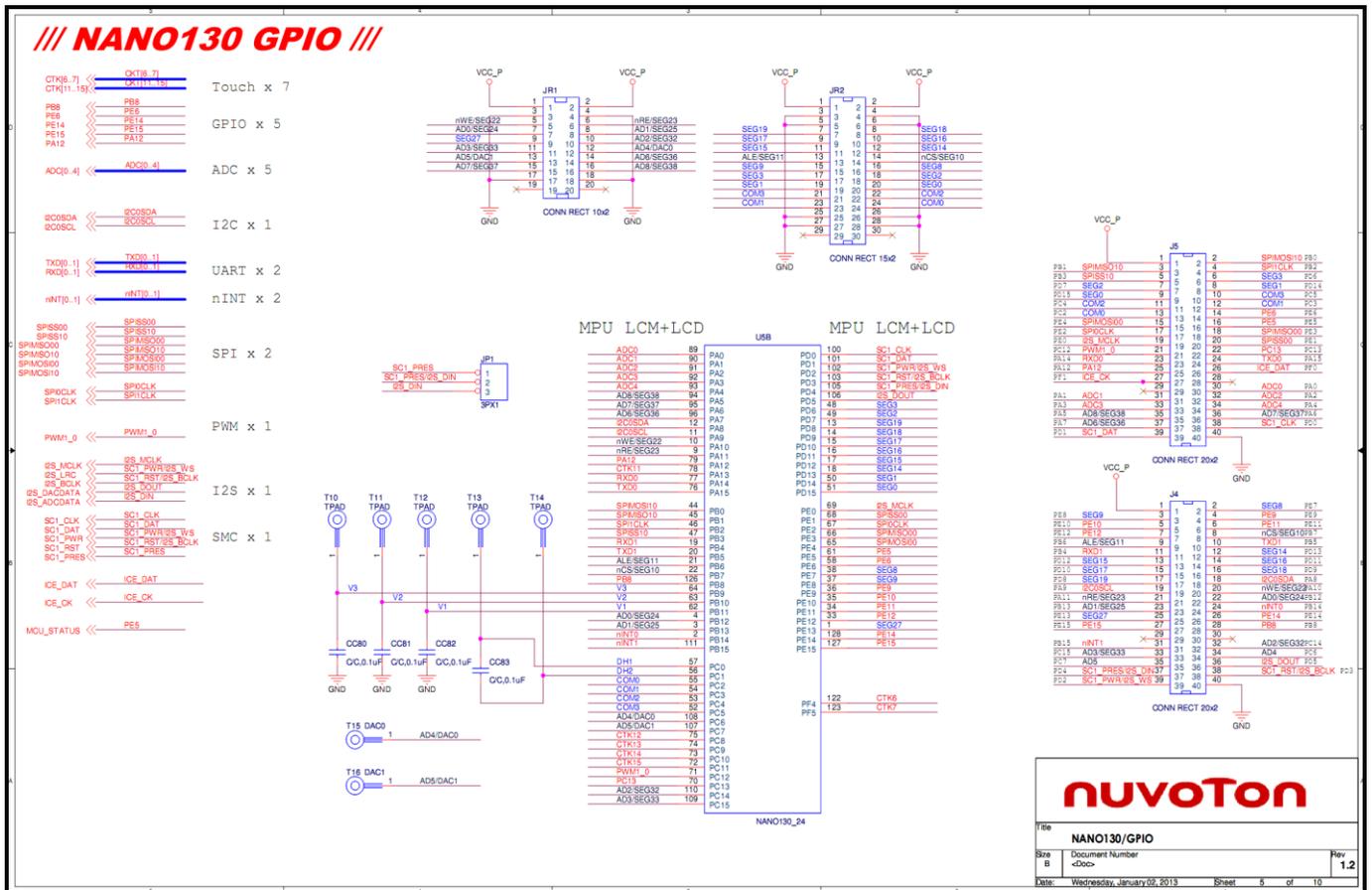
## 5. Sơ đồ mạch nguyên lý





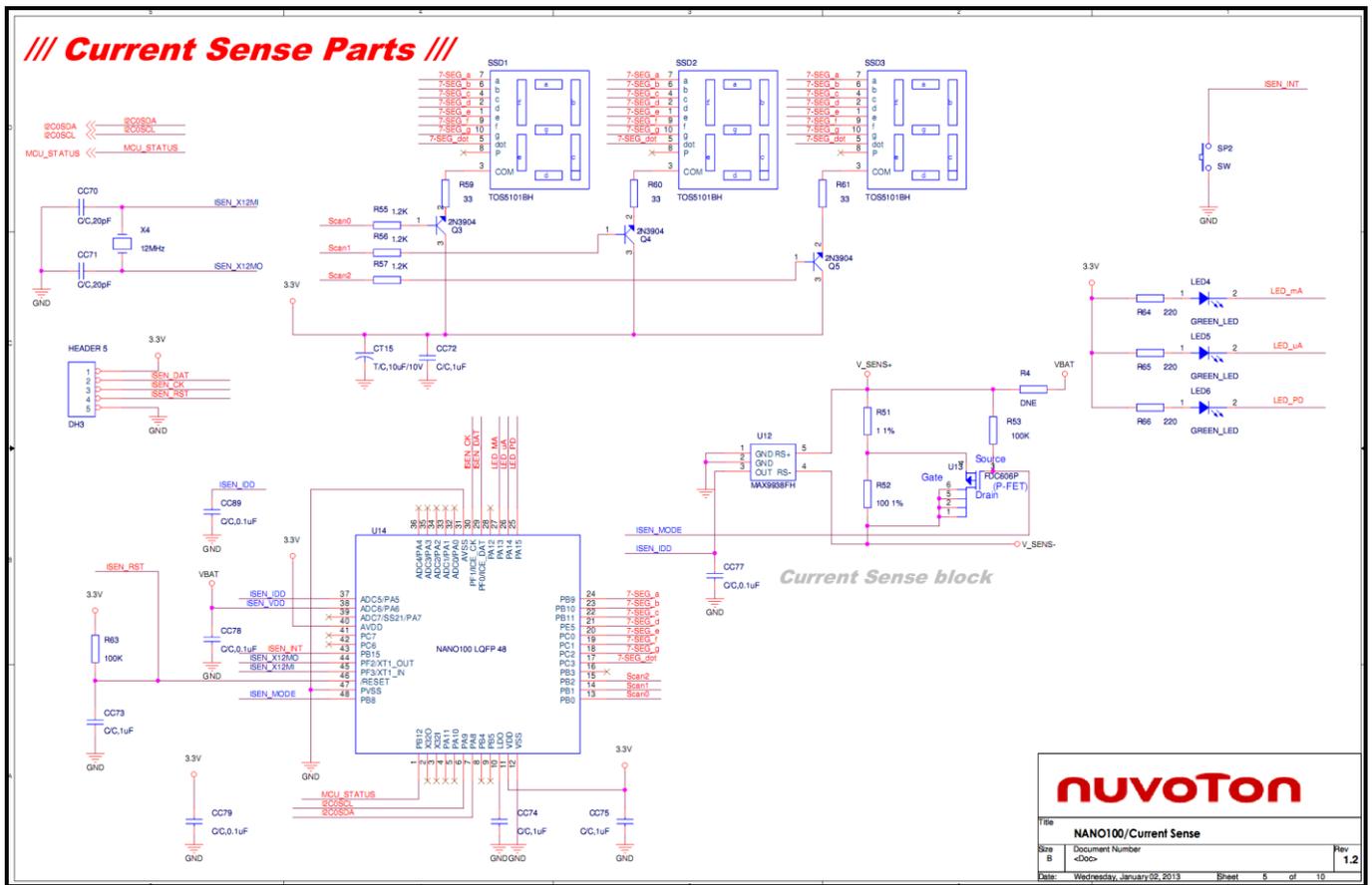


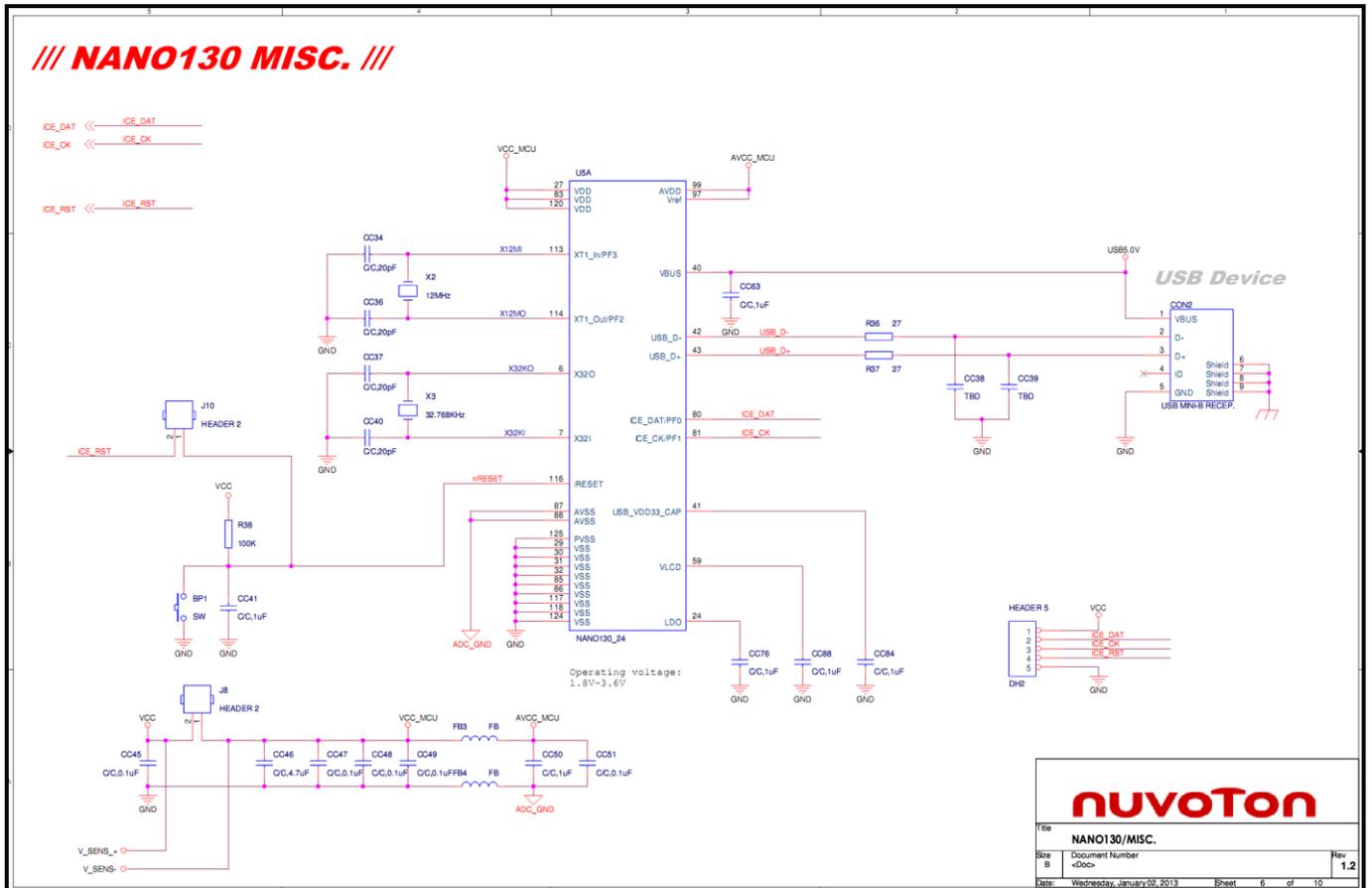


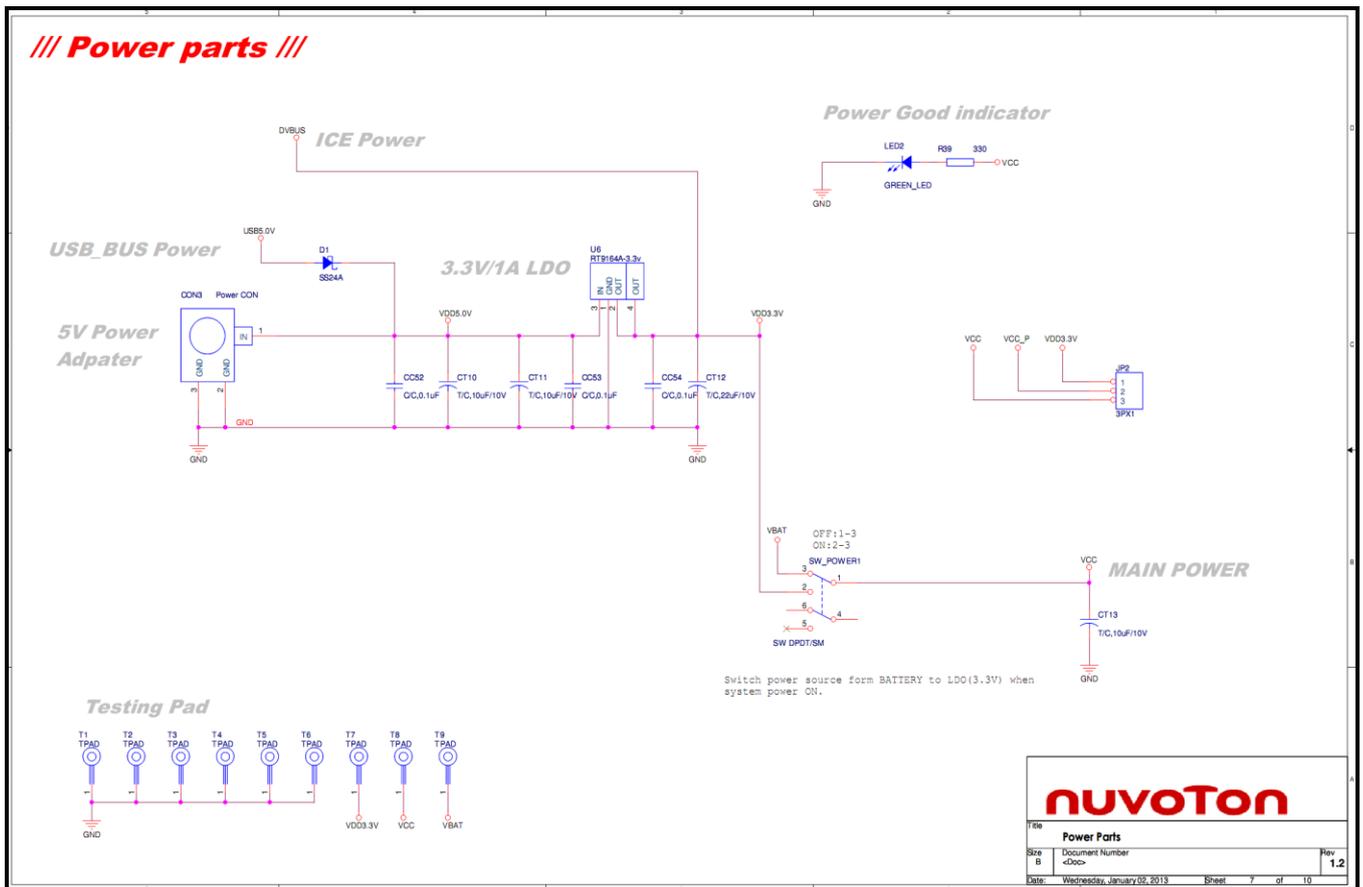


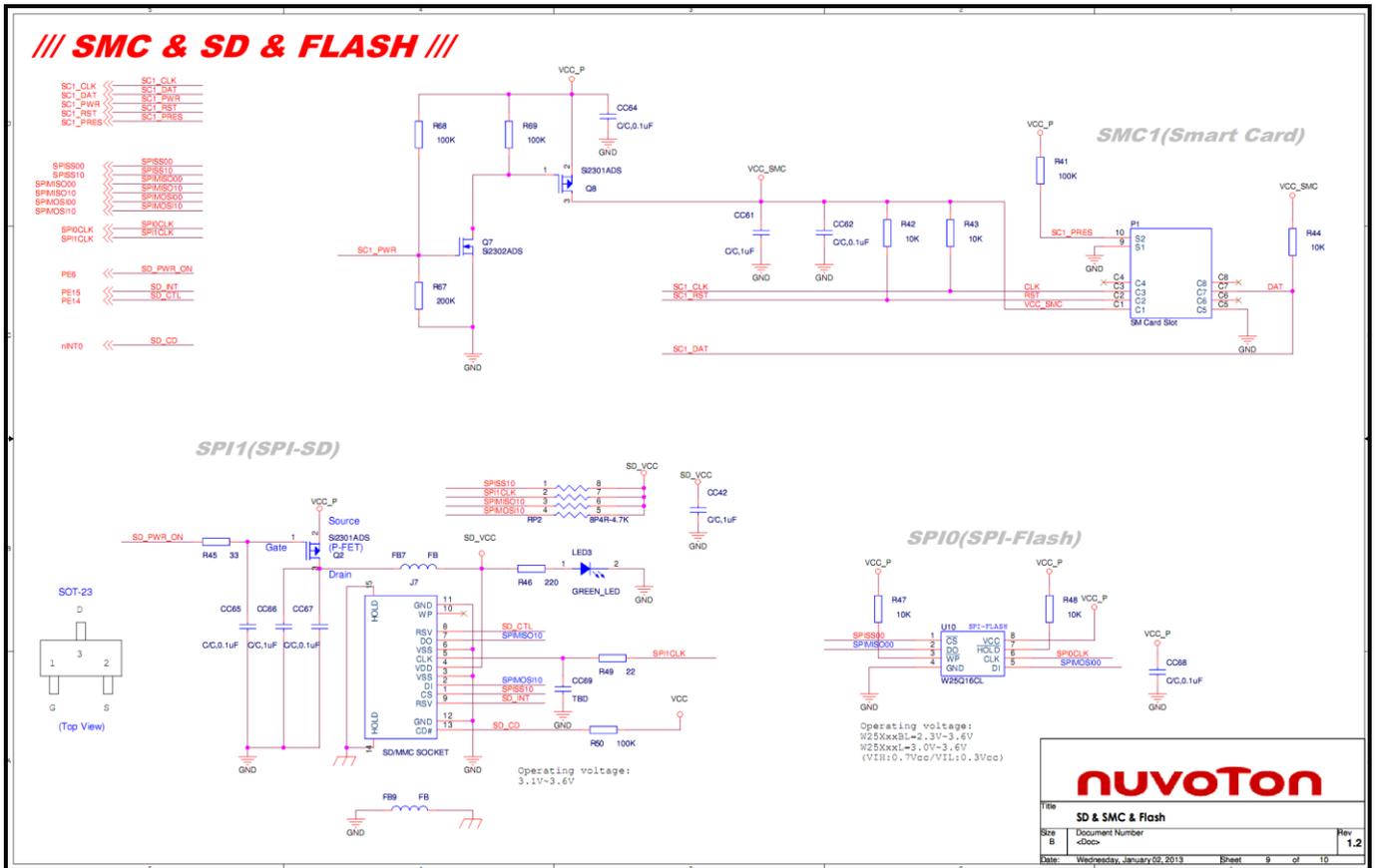

**nuvoton**

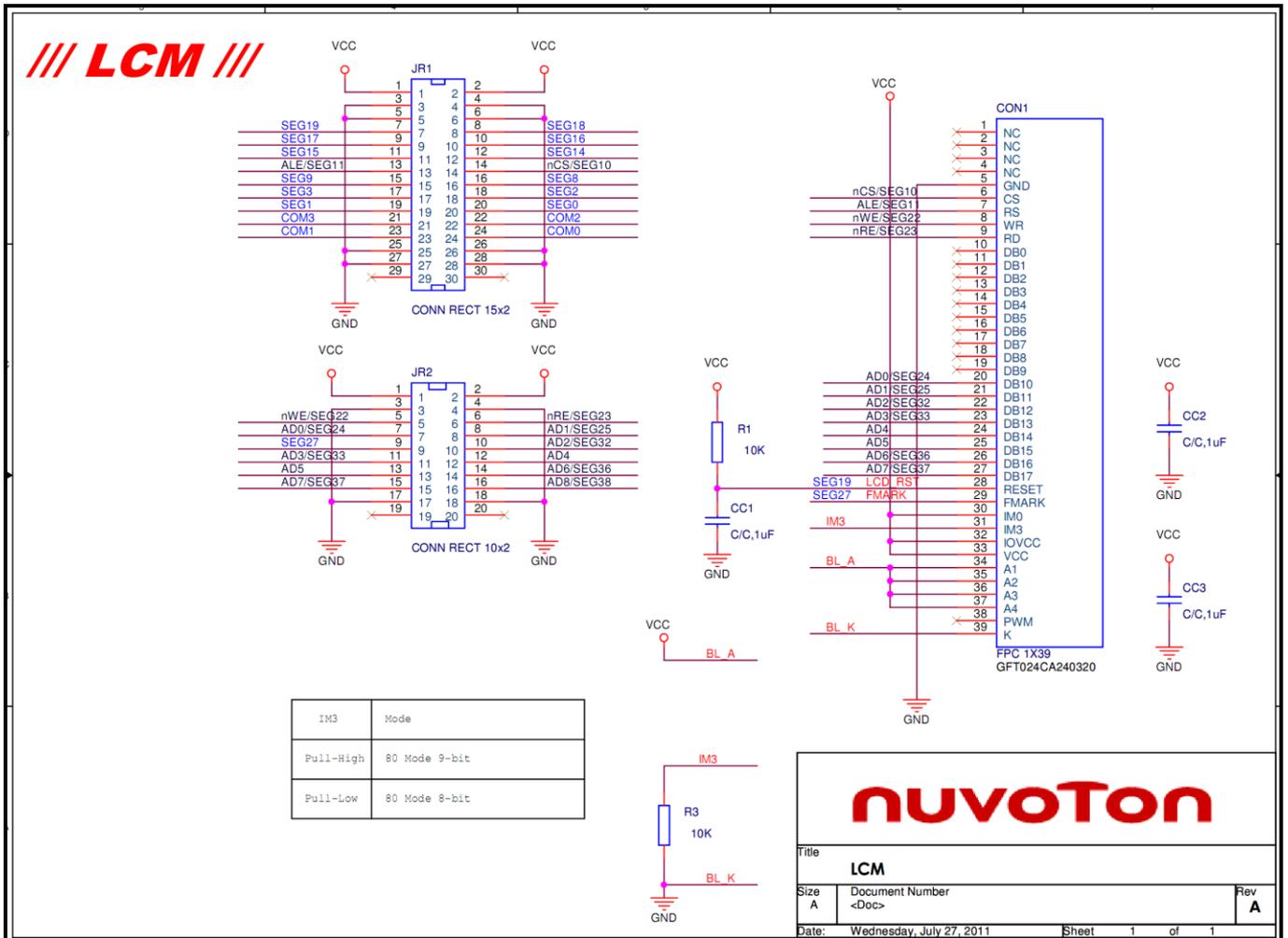
Title: NANO130/GPIO  
 Size: Document Number: Rev: 1.2  
 Date: Wednesday, January 02, 2013 Sheet: 5 of 10



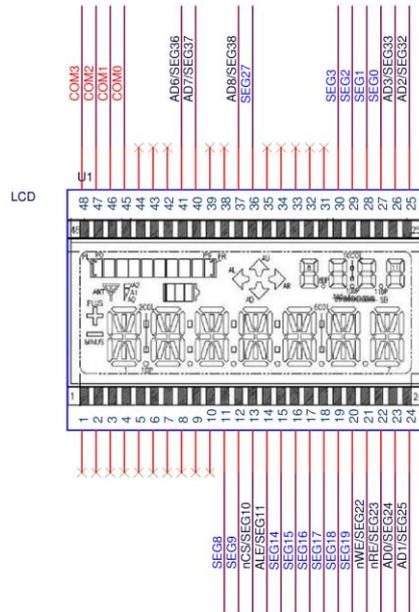
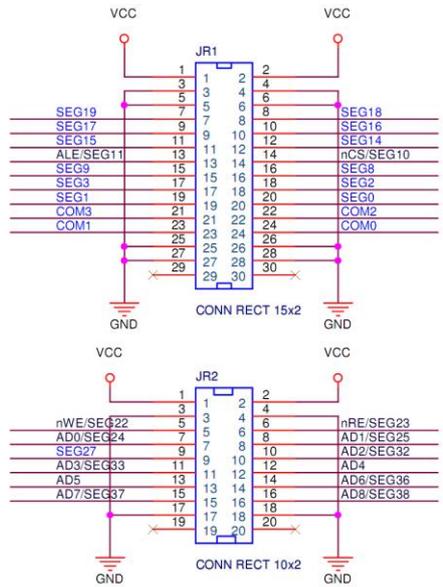








## /// LCD ///




Title	
LCD	
Size	Document Number
A	<Doc>
Date:	Monday, April 18, 2011
Sheet	1 of 1
Rev	A

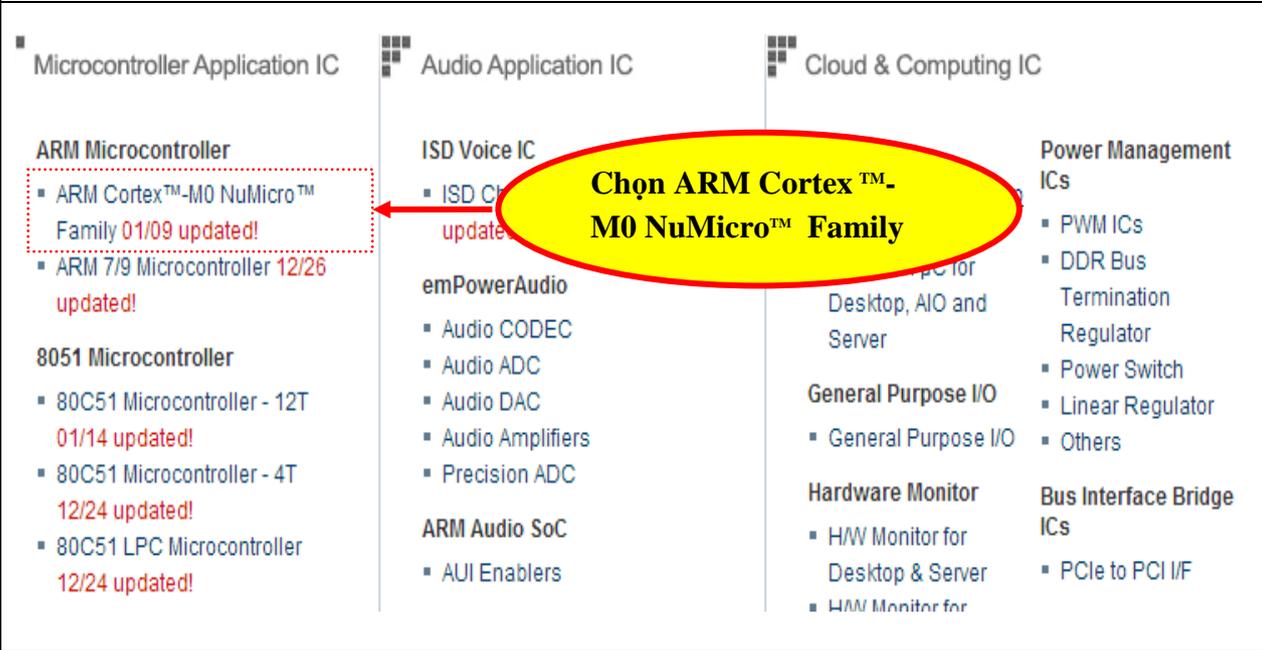
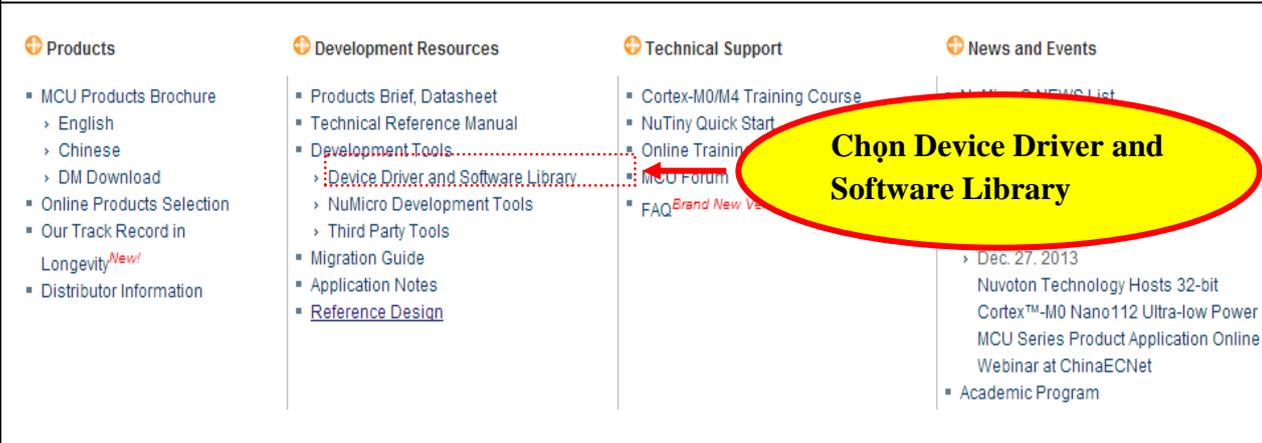
## 6. Công cụ hỗ trợ lập trình và phát triển

### 6.1 Công cụ hỗ trợ

Như các dòng ARM Cortex M0 khác của hãng Nuvoton như NUC100Series, M051, Mini51... để phát triển những ứng dụng sử dụng dòng Nano100Series(trong đó có Nano130) cần có:

- ✓ Môi trường ứng dụng phát triển(IDE): KeilC, IAR hoặc CooCox.
- ✓ Driver Nulink
- ✓ Thư viện hỗ trợ lập trình dòng Nano100 Series
- ✓ Phần mềm hỗ trợ nạp.

Tải các công cụ hỗ trợ, dựa theo hình ảnh:

Bước 1	Kết nối với trang chủ của công ty Nuvoton Website: <a href="http://www.nuvoton.com">http://www.nuvoton.com</a>
Bước 2	 <p>The screenshot shows the product categories on the Nuvoton website. A red dashed box highlights 'ARM Cortex™-M0 NuMicro™ Family 01/09 updated!'. A red arrow points from a yellow oval containing the text 'Chọn ARM Cortex™-M0 NuMicro™ Family' to this highlighted item.</p>
Bước 3	 <p>The screenshot shows the 'Development Resources' section of the Nuvoton website. A red dashed box highlights 'Device Driver and Software Library'. A red arrow points from a yellow oval containing the text 'Chọn Device Driver and Software Library' to this highlighted item.</p>

<p>Bước 4</p>	<p><b>Programmer Software Tools Package</b></p> <table border="1"> <thead> <tr> <th>File name</th> <th>Description</th> <th>Version</th> <th>Date</th> </tr> </thead> <tbody> <tr> <td> <a href="#">ICP Programming Tool V1.23.6103.zip</a>  <a href="#">Revision History</a> </td> <td>NuMicro ICP tool &amp; user manual</td> <td>V1.23.6103</td> <td>10-28-2013</td> </tr> <tr> <td> <a href="#">ISP Programming Tool V1.42.zip</a>  <a href="#">Revision History</a> </td> <td>NuMicro ISP tool &amp; user manual</td> <td>V1.42</td> <td>01-20-2012</td> </tr> <tr> <td> <a href="#">NuGang Programmer V6.19.zip</a>  <a href="#">Revision History</a> </td> <td>NuGang Programmer software &amp; user manual</td> <td>V6.19</td> <td>11-01-2012</td> </tr> </tbody> </table> <p><b>Phân mềm nạp chương trình</b></p> <p><b>Nu-Link Driver</b></p> <table border="1"> <thead> <tr> <th>File name</th> <th>Description</th> <th>Version</th> <th>Date</th> </tr> </thead> <tbody> <tr> <td> <a href="#">Nu-Link Driver for Keil RVMDK V1.23.6103.zip</a>  <a href="#">Revision History</a> </td> <td>This driver is to support Keil RVMDK Development Environment on NuMicro Family Devices.</td> <td></td> <td>10-28-2013</td> </tr> <tr> <td> <a href="#">Nu-Link Driver for IAR EWARM V1.23.6103.zip</a>  <a href="#">Revision History</a> </td> <td>This driver is to support IAR EWARM Development Environment on NuMicro Family Devices.</td> <td></td> <td>10-28-2013</td> </tr> </tbody> </table> <p><b>Driver hỗ trợ lập trình chip ARM Cortex M0 Nuvoton trên KeilC &amp; IAR</b></p> <p>Contact us: <a href="mailto:NuMicro@nuvoton.com">NuMicro@nuvoton.com</a></p>	File name	Description	Version	Date	<a href="#">ICP Programming Tool V1.23.6103.zip</a> <a href="#">Revision History</a>	NuMicro ICP tool & user manual	V1.23.6103	10-28-2013	<a href="#">ISP Programming Tool V1.42.zip</a> <a href="#">Revision History</a>	NuMicro ISP tool & user manual	V1.42	01-20-2012	<a href="#">NuGang Programmer V6.19.zip</a> <a href="#">Revision History</a>	NuGang Programmer software & user manual	V6.19	11-01-2012	File name	Description	Version	Date	<a href="#">Nu-Link Driver for Keil RVMDK V1.23.6103.zip</a> <a href="#">Revision History</a>	This driver is to support Keil RVMDK Development Environment on NuMicro Family Devices.		10-28-2013	<a href="#">Nu-Link Driver for IAR EWARM V1.23.6103.zip</a> <a href="#">Revision History</a>	This driver is to support IAR EWARM Development Environment on NuMicro Family Devices.		10-28-2013
File name	Description	Version	Date																										
<a href="#">ICP Programming Tool V1.23.6103.zip</a> <a href="#">Revision History</a>	NuMicro ICP tool & user manual	V1.23.6103	10-28-2013																										
<a href="#">ISP Programming Tool V1.42.zip</a> <a href="#">Revision History</a>	NuMicro ISP tool & user manual	V1.42	01-20-2012																										
<a href="#">NuGang Programmer V6.19.zip</a> <a href="#">Revision History</a>	NuGang Programmer software & user manual	V6.19	11-01-2012																										
File name	Description	Version	Date																										
<a href="#">Nu-Link Driver for Keil RVMDK V1.23.6103.zip</a> <a href="#">Revision History</a>	This driver is to support Keil RVMDK Development Environment on NuMicro Family Devices.		10-28-2013																										
<a href="#">Nu-Link Driver for IAR EWARM V1.23.6103.zip</a> <a href="#">Revision History</a>	This driver is to support IAR EWARM Development Environment on NuMicro Family Devices.		10-28-2013																										
<p>Bước 5</p>	<table border="1"> <tbody> <tr> <td> <a href="#">Nano100B Series CMSIS BSP_EN_V1.00.007.zip</a>  <a href="#">Revision History</a> </td> <td>           Nano100B series software package based on CMSIS version 3.1. It supports both development and production code for Nano100B series and Learning Board are included. For detailed, please download it and unzip it.         </td> <td></td> <td>11-2013</td> </tr> </tbody> </table> <p><b>Thư viện lập trình dòng Nano100 Series</b></p>	<a href="#">Nano100B Series CMSIS BSP_EN_V1.00.007.zip</a> <a href="#">Revision History</a>	Nano100B series software package based on CMSIS version 3.1. It supports both development and production code for Nano100B series and Learning Board are included. For detailed, please download it and unzip it.		11-2013																								
<a href="#">Nano100B Series CMSIS BSP_EN_V1.00.007.zip</a> <a href="#">Revision History</a>	Nano100B series software package based on CMSIS version 3.1. It supports both development and production code for Nano100B series and Learning Board are included. For detailed, please download it and unzip it.		11-2013																										
<p>Bước 6</p>	<table border="1"> <thead> <tr> <th>Products</th> <th>Development Resources</th> <th>Technical Support</th> <th>News and Events</th> </tr> </thead> <tbody> <tr> <td> <ul style="list-style-type: none"> <li>MCU Products Brochure               <ul style="list-style-type: none"> <li>English</li> <li>Chinese</li> </ul> </li> <li>DM Download</li> <li>Online Products Selection</li> <li>Our Track Record in Longevity <i>New!</i></li> <li>Distributor Information</li> </ul> </td> <td> <ul style="list-style-type: none"> <li>Products Brief, Datasheet</li> <li>Technical Reference Manual</li> <li>Development Tools               <ul style="list-style-type: none"> <li>Device Driver and Software Library</li> <li><b>NuMicro Development Tools</b></li> <li>Third Party Tools</li> </ul> </li> <li>Migration Guide</li> <li>Application Notes</li> <li>Reference Design</li> </ul> </td> <td> <ul style="list-style-type: none"> <li>Cortex-M0/M4 Training Course</li> <li>NuTiny Quick Start</li> <li>Online Training</li> <li>MCU Forum</li> <li>FAQ</li> </ul> </td> <td> <ul style="list-style-type: none"> <li>NuMicro@NEWS List               <ul style="list-style-type: none"> <li>Jul.31. 2013</li> </ul> </li> <li>NuMicro™ Family 32-bit New Series -</li> <li>Nuvoton Technology Hosts 32-bit Cortex™-M0 Nano112 Ultra-low Power MCU Series Product Application Online Webinar at ChinaECNet</li> <li>Academic Program</li> </ul> </td> </tr> </tbody> </table> <p><b>Chọn NuMicro Development Tools</b></p>	Products	Development Resources	Technical Support	News and Events	<ul style="list-style-type: none"> <li>MCU Products Brochure               <ul style="list-style-type: none"> <li>English</li> <li>Chinese</li> </ul> </li> <li>DM Download</li> <li>Online Products Selection</li> <li>Our Track Record in Longevity <i>New!</i></li> <li>Distributor Information</li> </ul>	<ul style="list-style-type: none"> <li>Products Brief, Datasheet</li> <li>Technical Reference Manual</li> <li>Development Tools               <ul style="list-style-type: none"> <li>Device Driver and Software Library</li> <li><b>NuMicro Development Tools</b></li> <li>Third Party Tools</li> </ul> </li> <li>Migration Guide</li> <li>Application Notes</li> <li>Reference Design</li> </ul>	<ul style="list-style-type: none"> <li>Cortex-M0/M4 Training Course</li> <li>NuTiny Quick Start</li> <li>Online Training</li> <li>MCU Forum</li> <li>FAQ</li> </ul>	<ul style="list-style-type: none"> <li>NuMicro@NEWS List               <ul style="list-style-type: none"> <li>Jul.31. 2013</li> </ul> </li> <li>NuMicro™ Family 32-bit New Series -</li> <li>Nuvoton Technology Hosts 32-bit Cortex™-M0 Nano112 Ultra-low Power MCU Series Product Application Online Webinar at ChinaECNet</li> <li>Academic Program</li> </ul>																				
Products	Development Resources	Technical Support	News and Events																										
<ul style="list-style-type: none"> <li>MCU Products Brochure               <ul style="list-style-type: none"> <li>English</li> <li>Chinese</li> </ul> </li> <li>DM Download</li> <li>Online Products Selection</li> <li>Our Track Record in Longevity <i>New!</i></li> <li>Distributor Information</li> </ul>	<ul style="list-style-type: none"> <li>Products Brief, Datasheet</li> <li>Technical Reference Manual</li> <li>Development Tools               <ul style="list-style-type: none"> <li>Device Driver and Software Library</li> <li><b>NuMicro Development Tools</b></li> <li>Third Party Tools</li> </ul> </li> <li>Migration Guide</li> <li>Application Notes</li> <li>Reference Design</li> </ul>	<ul style="list-style-type: none"> <li>Cortex-M0/M4 Training Course</li> <li>NuTiny Quick Start</li> <li>Online Training</li> <li>MCU Forum</li> <li>FAQ</li> </ul>	<ul style="list-style-type: none"> <li>NuMicro@NEWS List               <ul style="list-style-type: none"> <li>Jul.31. 2013</li> </ul> </li> <li>NuMicro™ Family 32-bit New Series -</li> <li>Nuvoton Technology Hosts 32-bit Cortex™-M0 Nano112 Ultra-low Power MCU Series Product Application Online Webinar at ChinaECNet</li> <li>Academic Program</li> </ul>																										

Bước 7

Nu-LB-NUC140		
Nu-LB-Nano130		

Contact us: [NuMicro@nuvoton.com](mailto:NuMicro@nuvoton.com)

**Mạch nguyên lý Board Nu-LB-Nano130**

Tải file Technical Reference Manual:



www.nuvoton.com/NuvotonMOSS/Community/ProductInfo.aspx?tp\_GUID=ca35dc89-c740-421a-b13b-5a8d050315e3

**NuMicro Family**

Home \ Product & Sales \ Product Lines \ Microcontroller Application IC \ ARM Microcontroller \ ARM Cortex™-M0 NuMicro™ Family

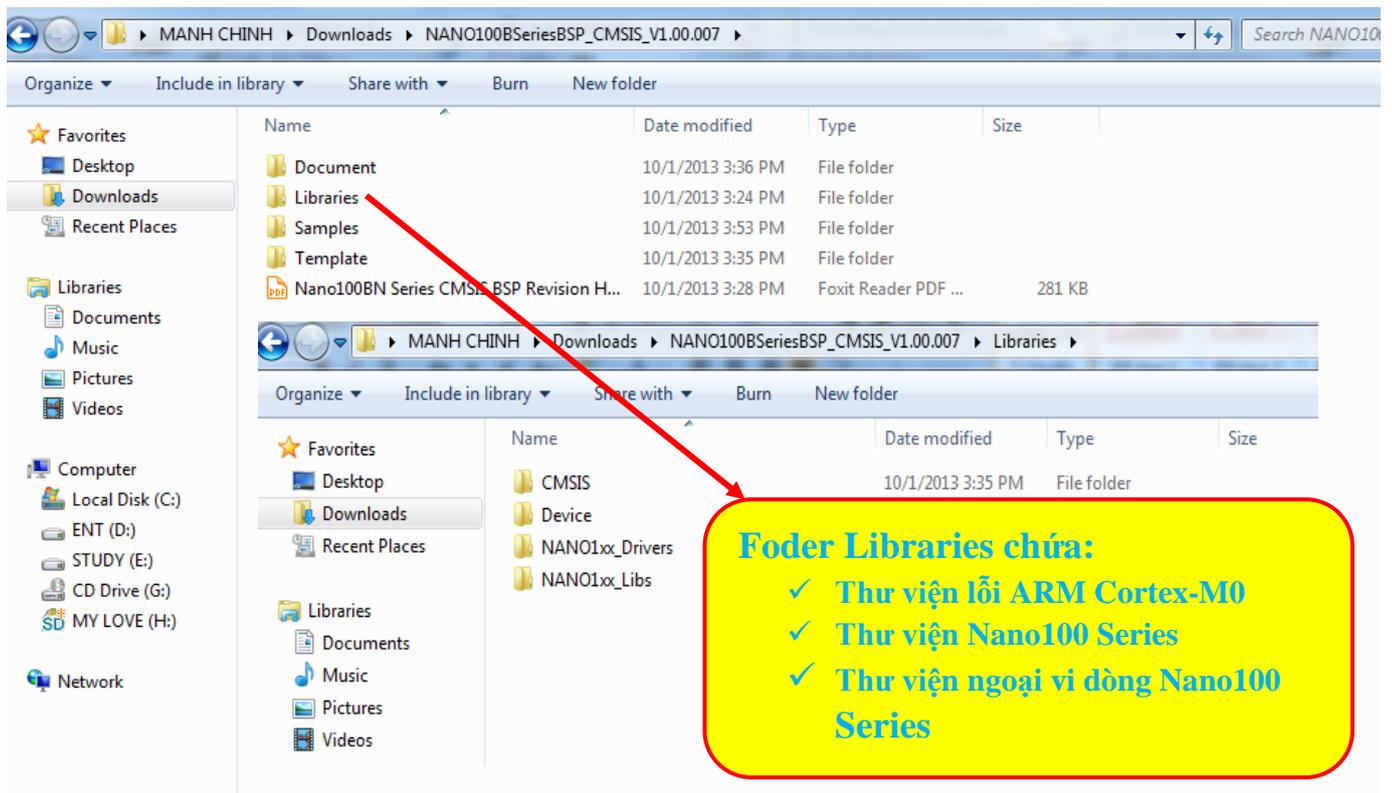
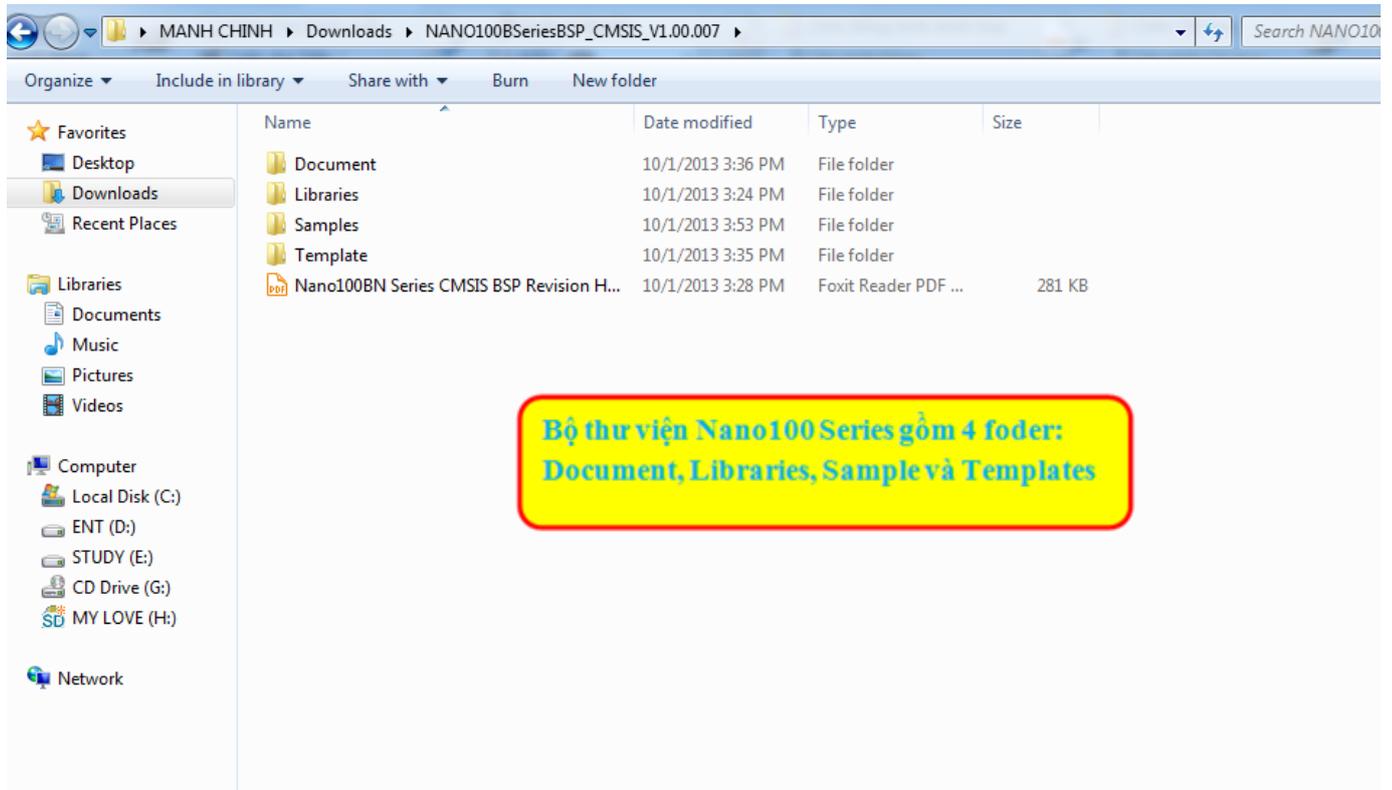
**Technical Reference Manual**

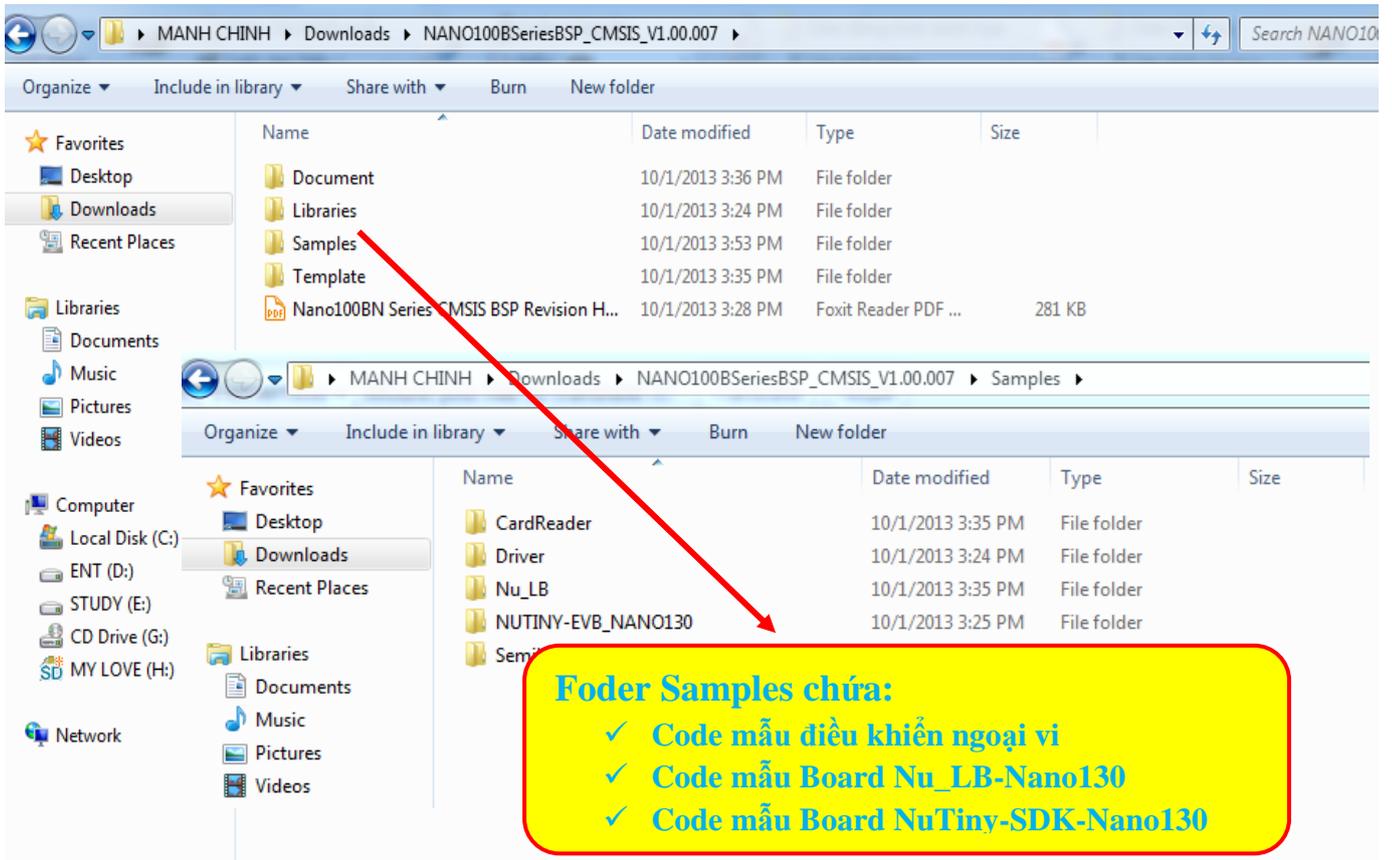
File name	Language	Version	Updated	Language	Version	Updated
Mini51 DE Technical Reference Manual V1.00	English	V1.00	10-31-2013	Chinese	-	-
M051 BN/DN/DE Series Technical Reference Manual V1.00	English	V1.00	09-17-2013	Chinese	-	-
M058S Technical Reference Manual V1.02	English	V1.02	11-06-2013	Chinese	-	-
NUC100 / 120 Technical Reference Manual V2.02	English	V2.02	01-16-2012	Chinese	V2.01	07-21-2011
NUC122 Technical Reference Manual V1.07	English	V1.07	06-27-2011	Chinese	V1.07	06-27-2011
NUC123 Technical Reference Manual V1.07	English	V1.07	03-29-2013	Chinese	V1.06	10-05-2012
NUC130 / 140 Technical Reference Manual V2.02	English	V2.02	01-19-2012	Chinese	V2.01	06-23-2011
NUC200 / 220 Technical Reference Manual V1.00	English	V1.00	12-07-2012	Chinese	-	-
<b>Nano100 BN Series Technical Reference Manual V1.07</b>	<b>English</b>	<b>V1.07</b>	<b>12-04-2013</b>	<b>Chinese</b>	<b>V1.07</b>	<b>12-04-2013</b>
AU9110 Technical Reference Manual V1.29	English	V1.29	11-07-2013	Chinese	-	-

Contact us: [NuMicro@nuvoton.com](mailto:NuMicro@nuvoton.com)

- ARM Video SoC
- Hardware Monitor
- Audio Enhancement
- Foundry Service
- Applications
- Solutions
- Technical Articles
- Worldwide Sales
- Product Reference
- Product Search
- RoHS Report

## Bộ thư viện dòng Nano100 Series

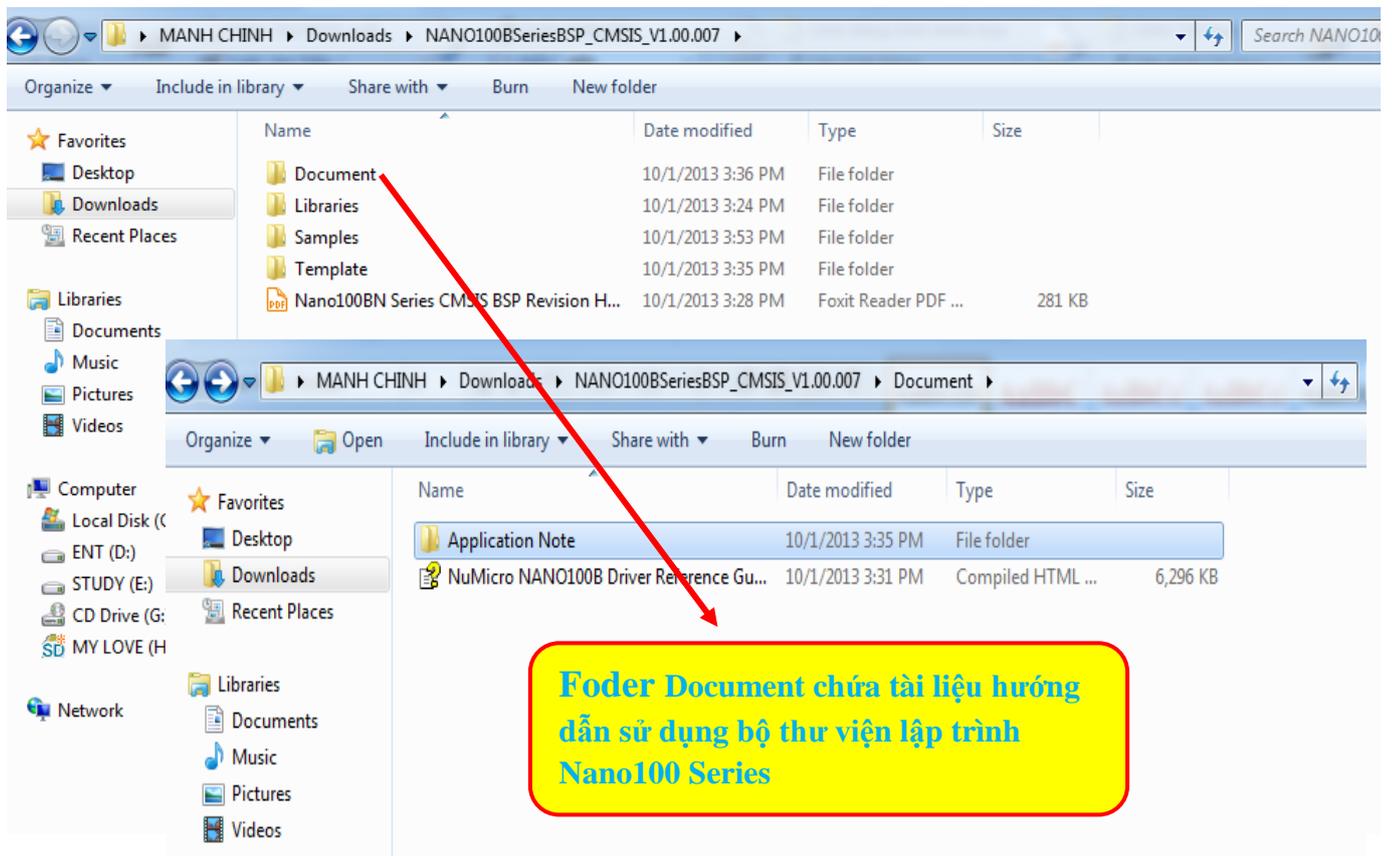




The screenshot shows two overlapping Windows Explorer windows. The top window displays the directory structure of the Nano100B Series BSP, including folders like Document, Libraries, Samples, and Template, and a PDF file. The bottom window shows the contents of the 'Samples' folder, which includes folders for CardReader, Driver, Nu\_LB, NUTINY-EVB\_NANO130, and Sem. A red arrow points from the 'Samples' folder in the top window to the 'Samples' folder in the bottom window. A yellow callout box with a red border highlights the contents of the 'Samples' folder.

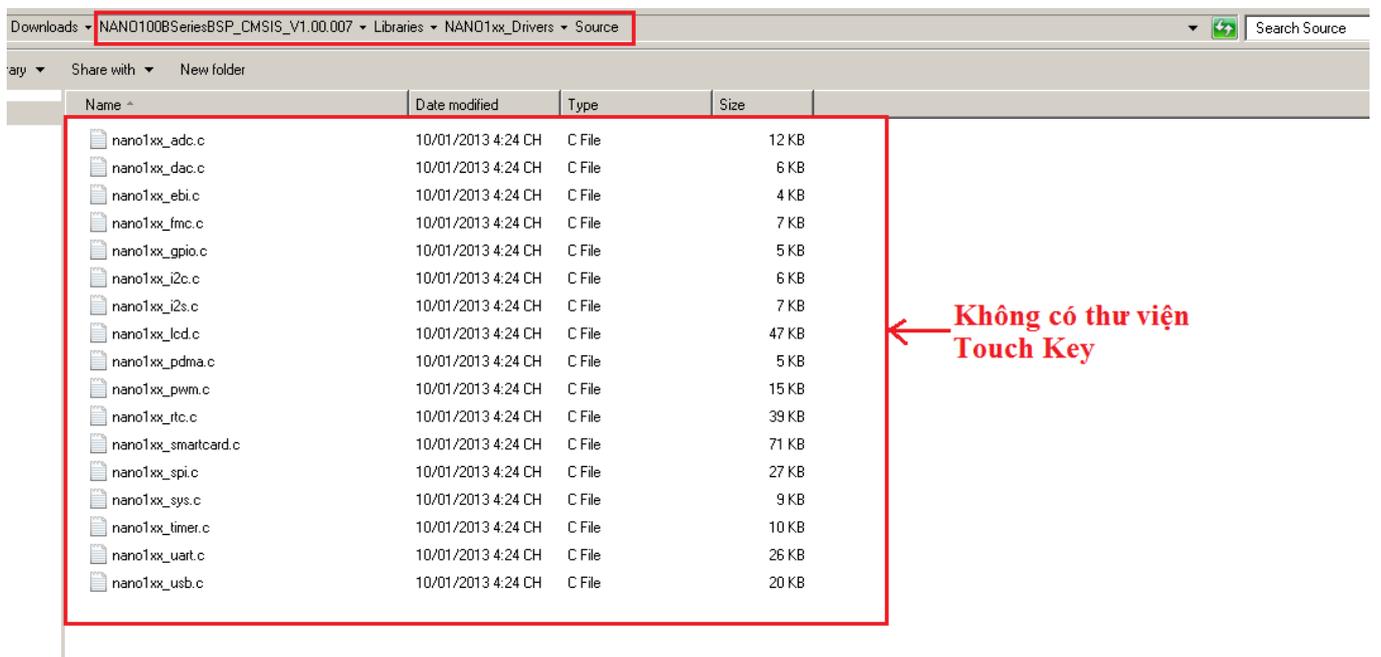
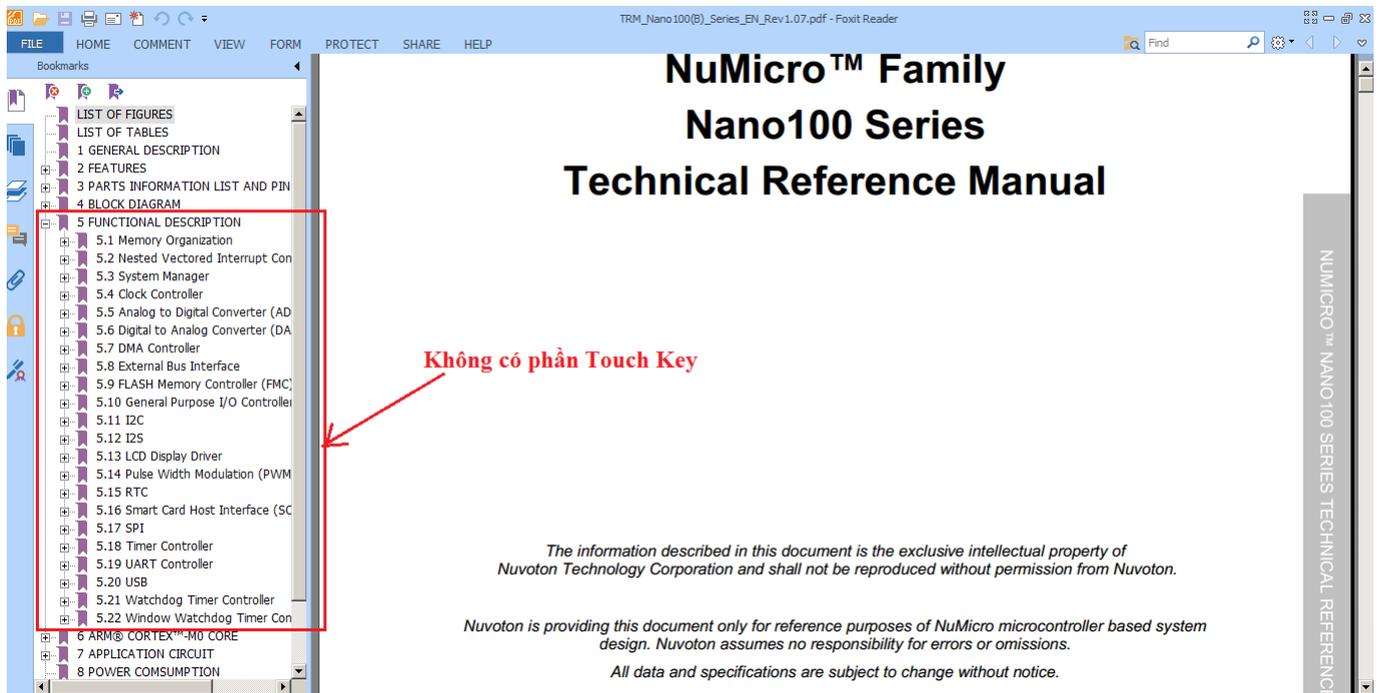
**Foder Samples chứa:**

- ✓ Code mẫu điều khiển ngoại vi
- ✓ Code mẫu Board Nu\_LB-Nano130
- ✓ Code mẫu Board NuTiny-SDK-Nano130



## 6.2 Bổ sung và chỉnh sửa tài liệu

Bộ thư viện thư viện lập trình dòng Nano (NANO100BSeriesBSP\_CMSIS\_V1.00.007) và tài liệu Technical Reference Manual tải trên trang chủ phía trên chưa cập nhật thư viện hỗ trợ giao tiếp cảm ứng Touch Key

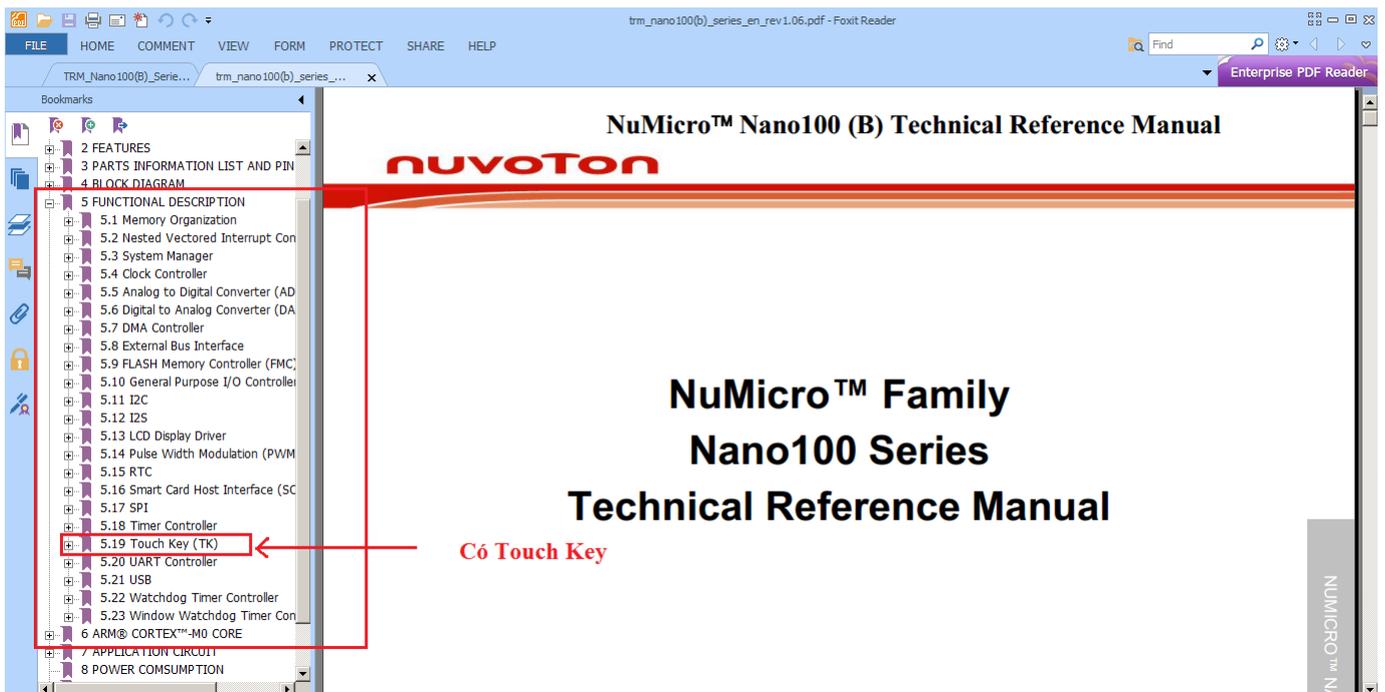


Để bổ sung thêm tính năng Touch Key làm theo các bước sau:

**Bước 1: Tải tài liệu bổ sung**

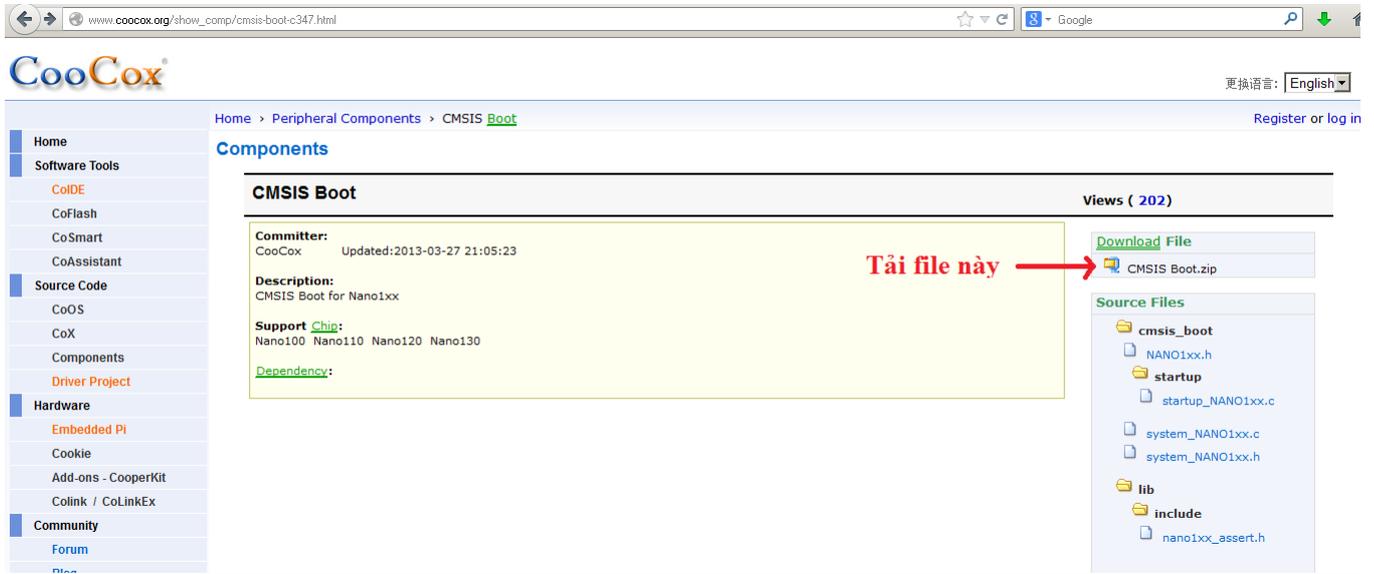
\_ Tải tài liệu Technical Reference(có Touch Key) theo đường dẫn sau:

<http://www.keil.com/dd/chip/7148.htm>



\_ Tải thư viện Nano130 Series theo đường dẫn

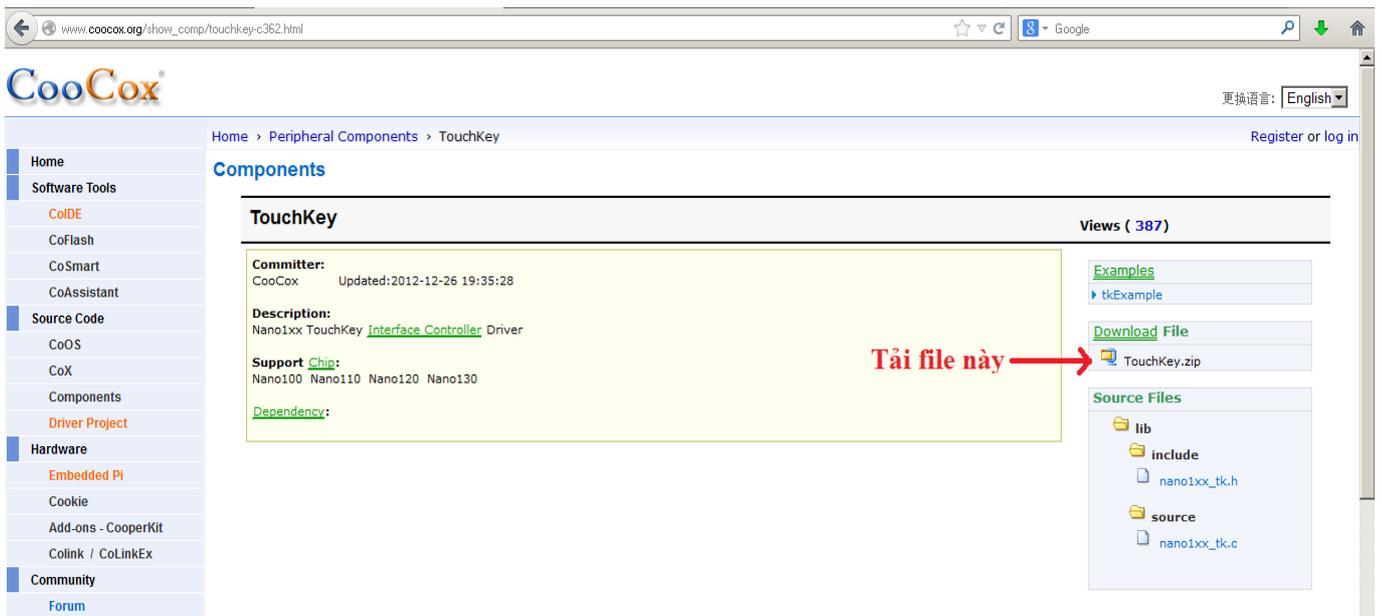
[http://www.cocox.org/show\\_comp/cmsis-boot-c347.html](http://www.cocox.org/show_comp/cmsis-boot-c347.html)



The screenshot shows the Cocox website interface for the CMSIS Boot component. The page title is "CMSIS Boot" and it has 202 views. The component details include: Committer: CoCox, Updated: 2013-03-27 21:05:23; Description: CMSIS Boot for Nano1xx; Support Chip: Nano100, Nano110, Nano120, Nano130; and Dependency: (empty). A red arrow points from the text "Tải file này" to the "Download File" button, which is labeled "CMSIS Boot.zip". The "Source Files" section lists: cmsis\_boot, NANO1xx.h, startup, startup\_NANO1xx.c, system\_NANO1xx.c, system\_NANO1xx.h, lib, include, and nano1xx\_assert.h.

\_ Tải thư viện Touch Key theo đường dẫn

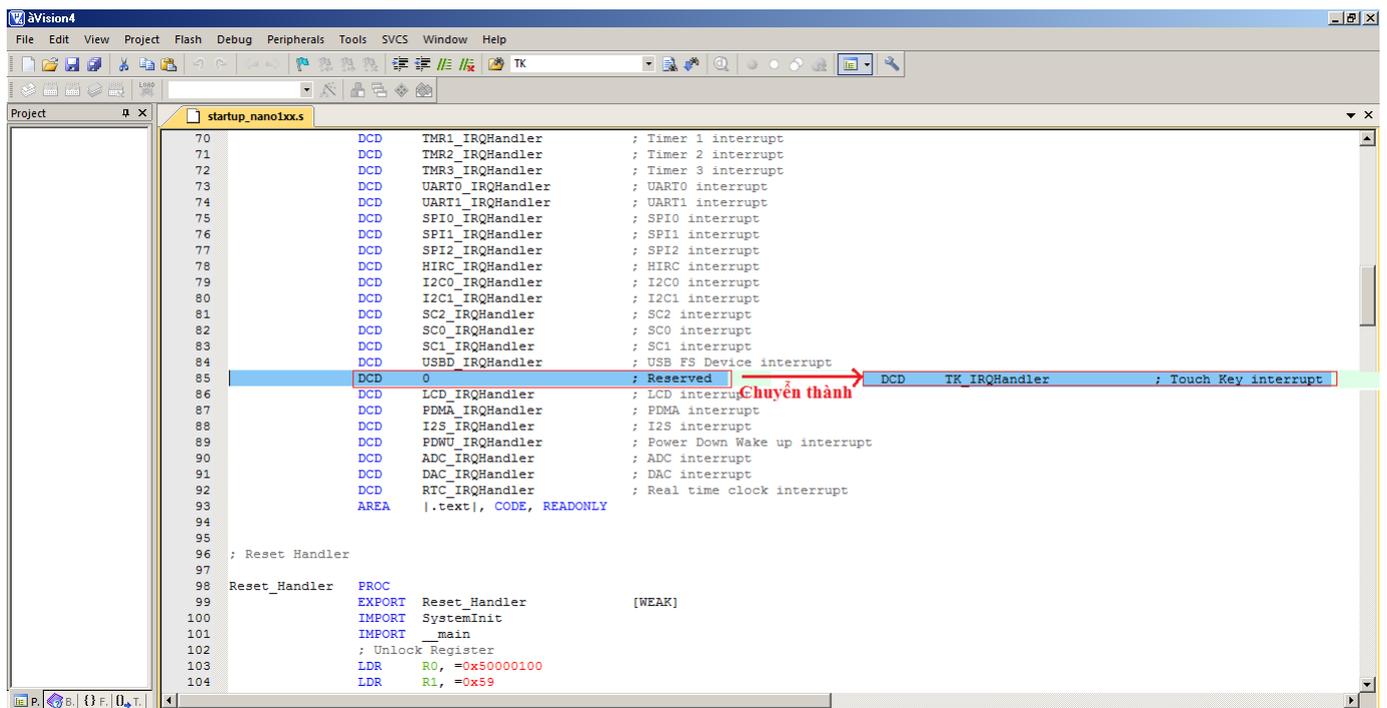
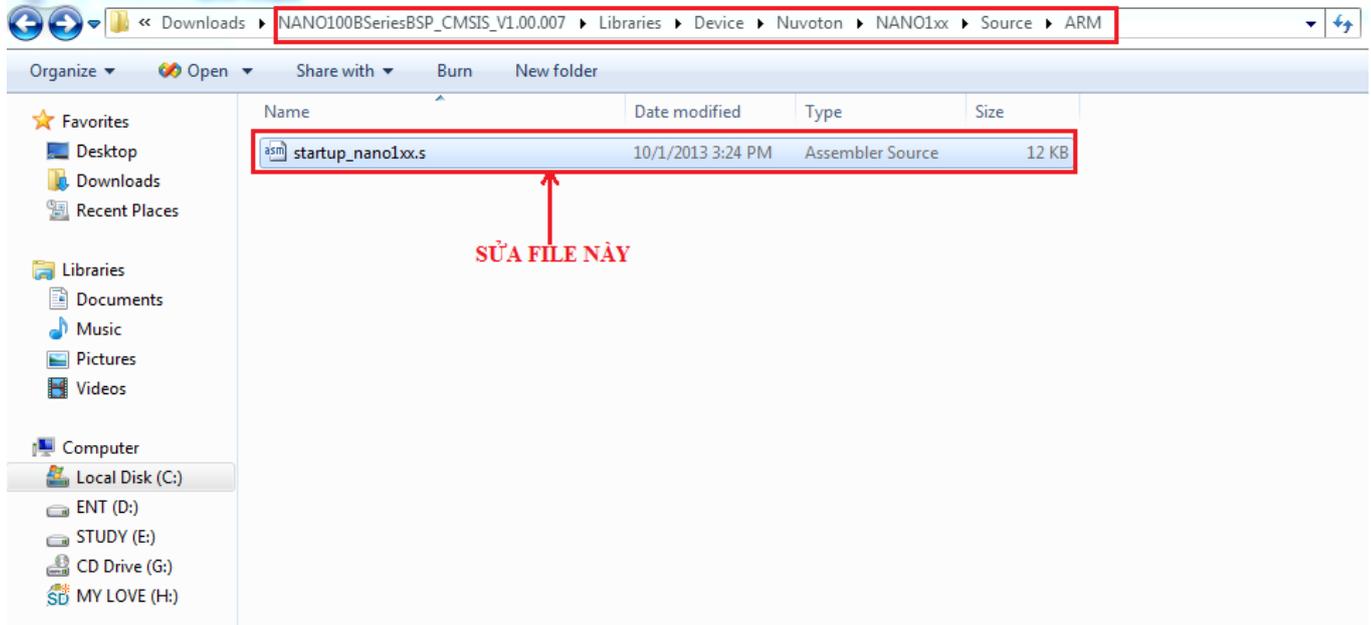
[http://www.cocox.org/show\\_comp/touchkey-c362.html](http://www.cocox.org/show_comp/touchkey-c362.html)

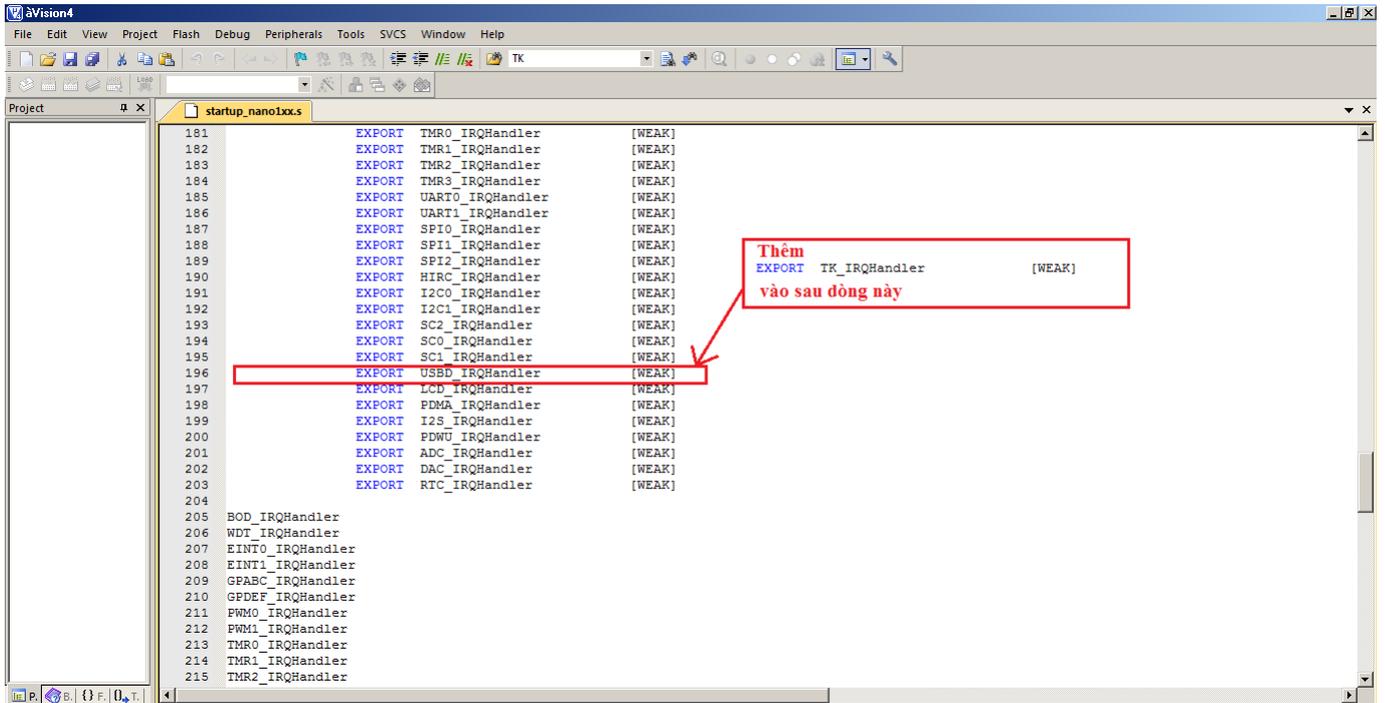


The screenshot shows the Cocox website interface for the TouchKey component. The page title is "TouchKey" and it has 387 views. The component details include: Committer: CoCox, Updated: 2012-12-26 19:35:28; Description: Nano1xx TouchKey [Interface Controller](#) Driver; Support Chip: Nano100, Nano110, Nano120, Nano130; and Dependency: (empty). A red arrow points from the text "Tải file này" to the "Download File" button, which is labeled "TouchKey.zip". The "Source Files" section lists: lib, include, nano1xx\_tk.h, source, and nano1xx\_tk.c.

Bước 2: Sửa file *startup\_nano1xx.s* trong thư viện

Mở file *startup\_nano1xx.s* như hình dưới:



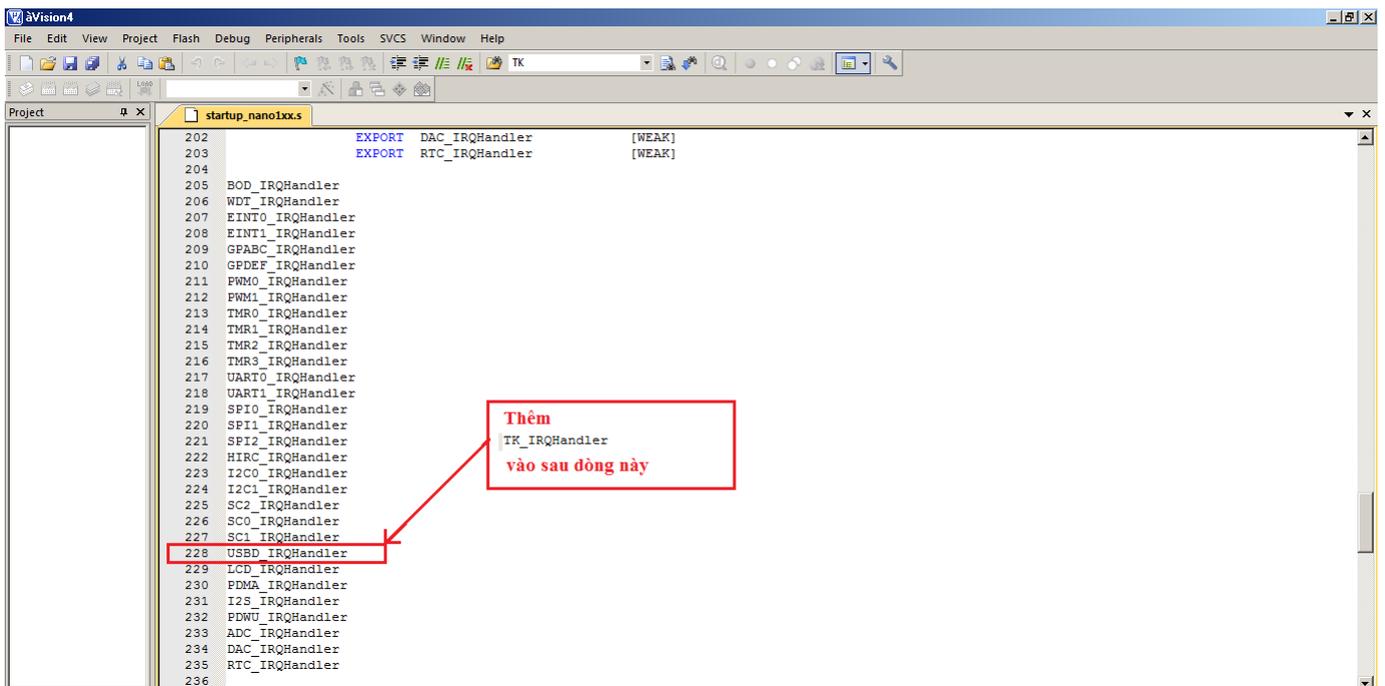


```

181 EXPORT TMR0_IRQHandler [WEAK]
182 EXPORT TMR1_IRQHandler [WEAK]
183 EXPORT TMR2_IRQHandler [WEAK]
184 EXPORT TMR3_IRQHandler [WEAK]
185 EXPORT UART0_IRQHandler [WEAK]
186 EXPORT UART1_IRQHandler [WEAK]
187 EXPORT SPI0_IRQHandler [WEAK]
188 EXPORT SPI1_IRQHandler [WEAK]
189 EXPORT SPI2_IRQHandler [WEAK]
190 EXPORT HIRC_IRQHandler [WEAK]
191 EXPORT I2C0_IRQHandler [WEAK]
192 EXPORT I2C1_IRQHandler [WEAK]
193 EXPORT SC2_IRQHandler [WEAK]
194 EXPORT SC0_IRQHandler [WEAK]
195 EXPORT SC1_IRQHandler [WEAK]
196 EXPORT USB_D_IRQHandler [WEAK]
197 EXPORT LCD_IRQHandler [WEAK]
198 EXPORT PDMA_IRQHandler [WEAK]
199 EXPORT I2S_IRQHandler [WEAK]
200 EXPORT PDWU_IRQHandler [WEAK]
201 EXPORT ADC_IRQHandler [WEAK]
202 EXPORT DAC_IRQHandler [WEAK]
203 EXPORT RTC_IRQHandler [WEAK]
204
205 BOD_IRQHandler
206 WDT_IRQHandler
207 EINT0_IRQHandler
208 EINT1_IRQHandler
209 GPABC_IRQHandler
210 GPDEF_IRQHandler
211 PWM0_IRQHandler
212 PWM1_IRQHandler
213 TMR0_IRQHandler
214 TMR1_IRQHandler
215 TMR2_IRQHandler

```

Thêm  
EXPORT TK\_IRQHandler [WEAK]  
vào sau dòng này



```

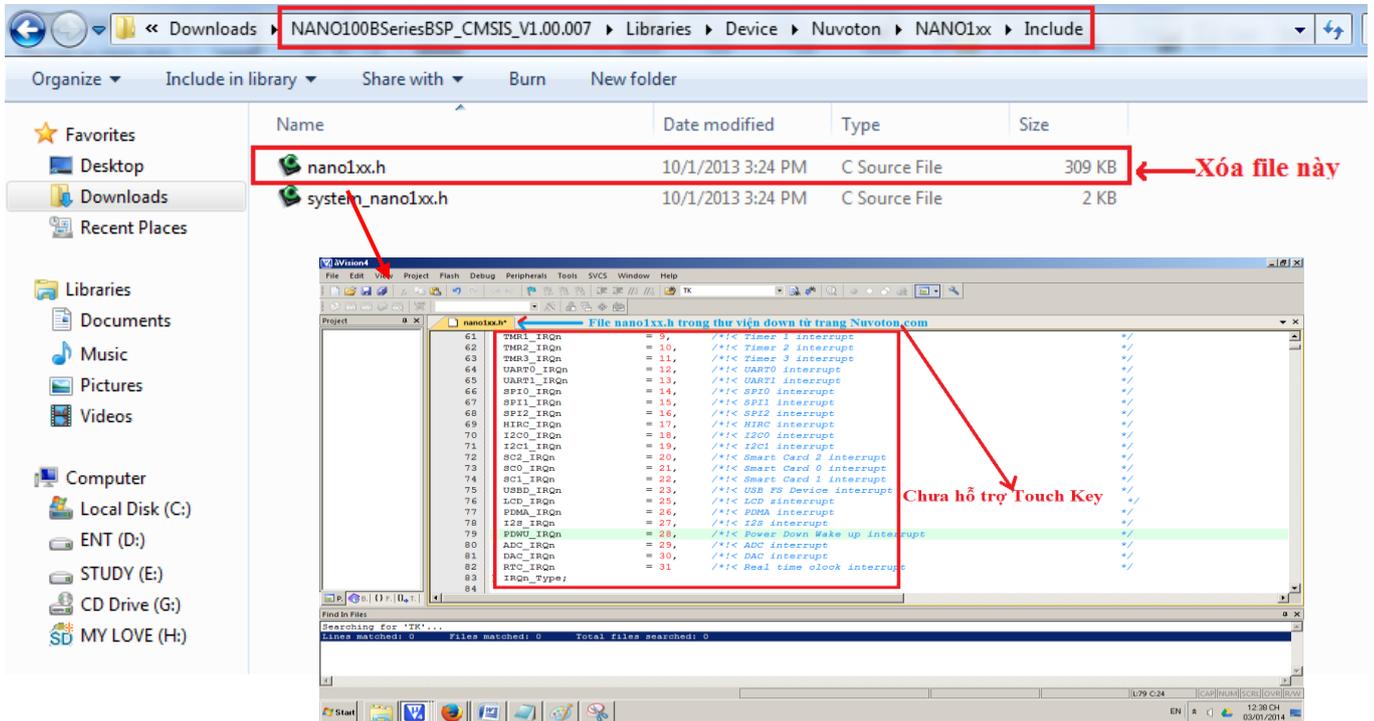
202 EXPORT DAC_IRQHandler [WEAK]
203 EXPORT RTC_IRQHandler [WEAK]
204
205 BOD_IRQHandler
206 WDT_IRQHandler
207 EINT0_IRQHandler
208 EINT1_IRQHandler
209 GPABC_IRQHandler
210 GPDEF_IRQHandler
211 PWM0_IRQHandler
212 PWM1_IRQHandler
213 TMR0_IRQHandler
214 TMR1_IRQHandler
215 TMR2_IRQHandler
216 TMR3_IRQHandler
217 UART0_IRQHandler
218 UART1_IRQHandler
219 SPI0_IRQHandler
220 SPI1_IRQHandler
221 SPI2_IRQHandler
222 HIRC_IRQHandler
223 I2C0_IRQHandler
224 I2C1_IRQHandler
225 SC2_IRQHandler
226 SC0_IRQHandler
227 SC1_IRQHandler
228 USB_D_IRQHandler
229 LCD_IRQHandler
230 PDMA_IRQHandler
231 I2S_IRQHandler
232 PDWU_IRQHandler
233 ADC_IRQHandler
234 DAC_IRQHandler
235 RTC_IRQHandler
236

```

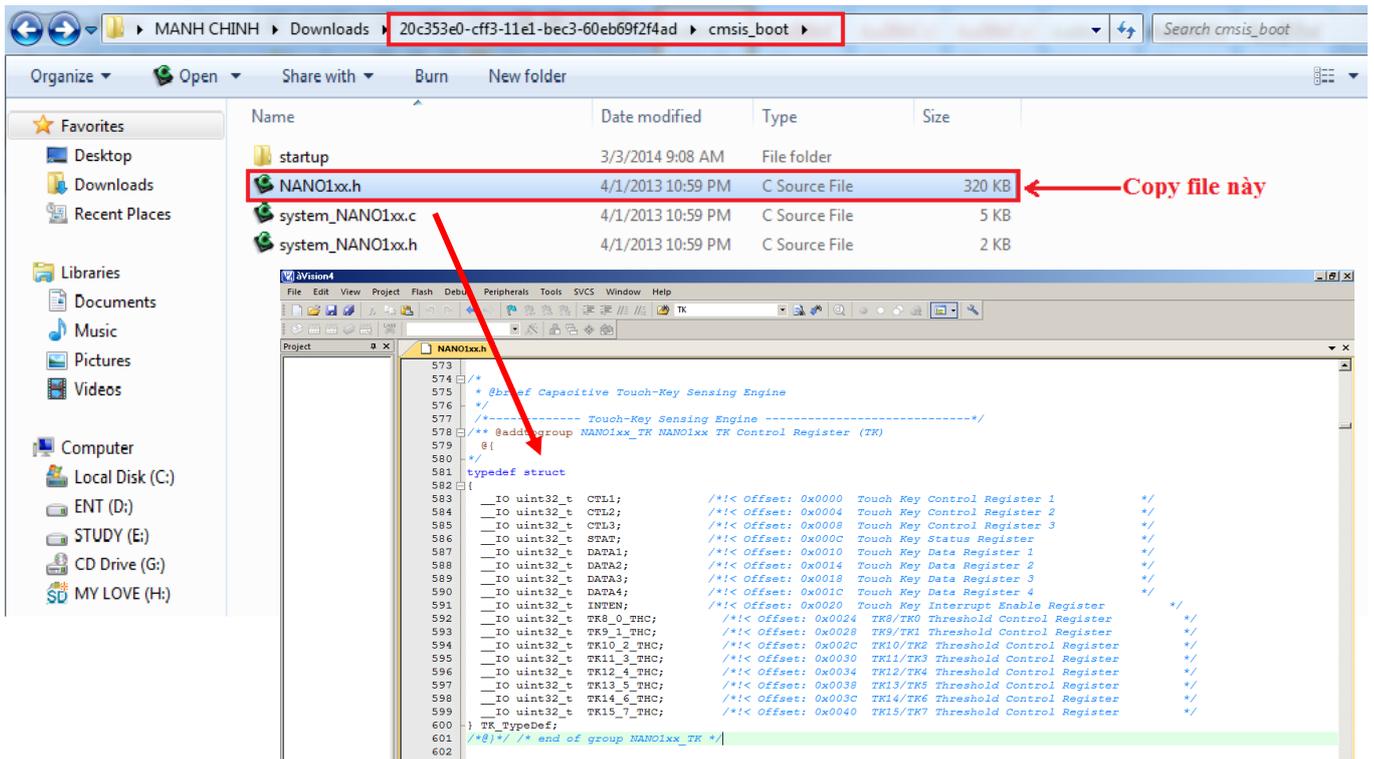
Thêm  
TK\_IRQHandler  
vào sau dòng này

### Bước 3: Sửa file *nano1xx.h* trong thư viện

Xóa file *nano1xx.h* theo đường dẫn như hình dưới đây

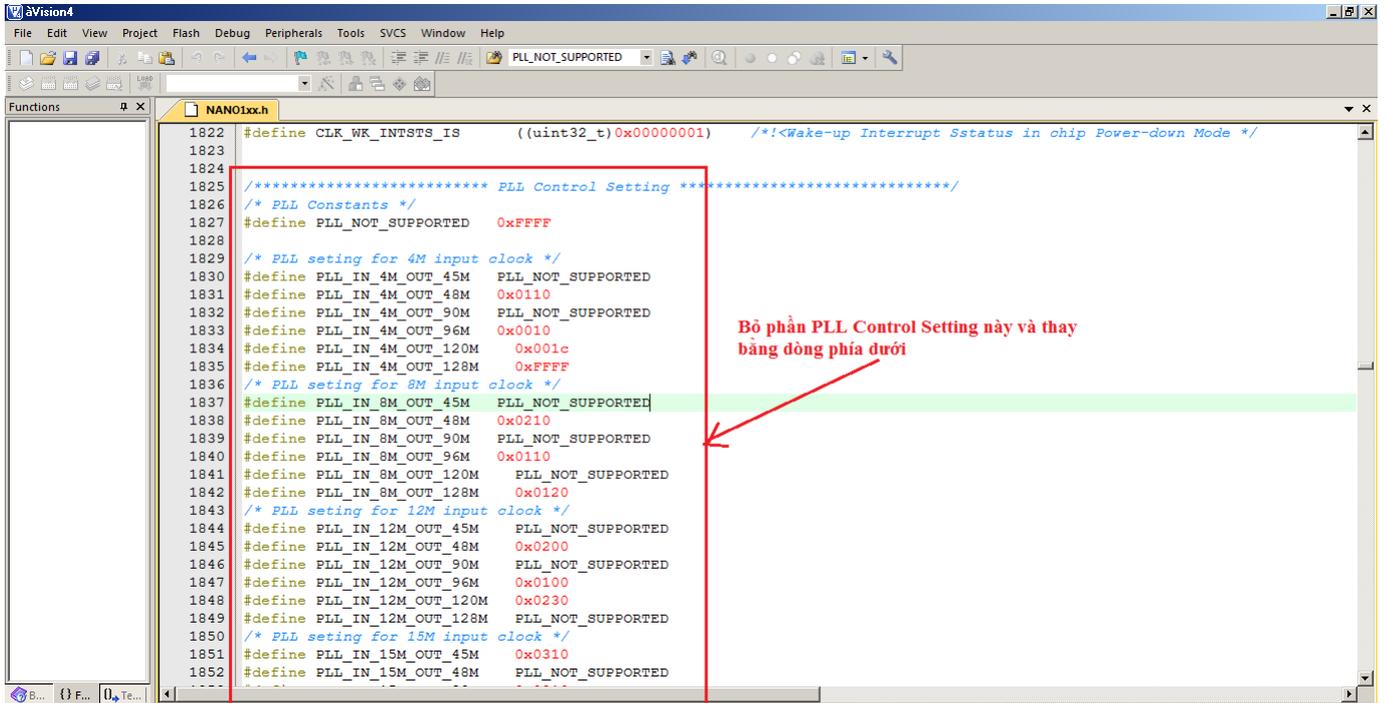


Sau đó copy file *NANO1xx.h* vừa mới tải về vào



Mở file NANO1xx.h vừa copy lên và chỉnh như sau:

\_ Xóa phần PLL Control Setting



```

1822 #define CLK_WK_INTSTS_IS ((uint32_t)0x00000001) /*!Wake-up Interrupt Sstatus in chip Power-down Mode */
1823
1824
1825 /****** PLL Control Setting *****/
1826 /* PLL Constants */
1827 #define PLL_NOT_SUPPORTED 0xFFFF
1828
1829 /* PLL setting for 4M input clock */
1830 #define PLL_IN_4M_OUT_45M PLL_NOT_SUPPORTED
1831 #define PLL_IN_4M_OUT_48M 0x0110
1832 #define PLL_IN_4M_OUT_90M PLL_NOT_SUPPORTED
1833 #define PLL_IN_4M_OUT_96M 0x0010
1834 #define PLL_IN_4M_OUT_120M 0x001c
1835 #define PLL_IN_4M_OUT_128M 0xFFFF
1836 /* PLL setting for 8M input clock */
1837 #define PLL_IN_8M_OUT_45M PLL_NOT_SUPPORTED
1838 #define PLL_IN_8M_OUT_48M 0x0210
1839 #define PLL_IN_8M_OUT_90M PLL_NOT_SUPPORTED
1840 #define PLL_IN_8M_OUT_96M 0x0110
1841 #define PLL_IN_8M_OUT_120M PLL_NOT_SUPPORTED
1842 #define PLL_IN_8M_OUT_128M 0x0120
1843 /* PLL setting for 12M input clock */
1844 #define PLL_IN_12M_OUT_45M PLL_NOT_SUPPORTED
1845 #define PLL_IN_12M_OUT_48M 0x0200
1846 #define PLL_IN_12M_OUT_90M PLL_NOT_SUPPORTED
1847 #define PLL_IN_12M_OUT_96M 0x0100
1848 #define PLL_IN_12M_OUT_120M 0x0230
1849 #define PLL_IN_12M_OUT_128M PLL_NOT_SUPPORTED
1850 /* PLL setting for 15M input clock */
1851 #define PLL_IN_15M_OUT_45M 0x0310
1852 #define PLL_IN_15M_OUT_48M PLL_NOT_SUPPORTED

```

Và thay bằng khối sau:

```

/***** PLL Control Setting *****/
/* PLL Constants */
#define PLL_NOT_SUPPORTED 0xFFFF

/* PLL setting for 4M input clock */
#define PLL_IN_4M_OUT_42M 0x010A
#define PLL_IN_4M_OUT_45M PLL_NOT_SUPPORTED
#define PLL_IN_4M_OUT_48M 0x0110
#define PLL_IN_4M_OUT_84M 0x000A
#define PLL_IN_4M_OUT_90M PLL_NOT_SUPPORTED
#define PLL_IN_4M_OUT_96M 0x0010
#define PLL_IN_4M_OUT_120M 0x001c
#define PLL_IN_4M_OUT_128M PLL_NOT_SUPPORTED
/* PLL setting for 8M input clock */
#define PLL_IN_8M_OUT_42M 0x020A
#define PLL_IN_8M_OUT_45M PLL_NOT_SUPPORTED
#define PLL_IN_8M_OUT_48M 0x0210
#define PLL_IN_8M_OUT_84M 0x010A
#define PLL_IN_8M_OUT_90M PLL_NOT_SUPPORTED
#define PLL_IN_8M_OUT_96M 0x0110
#define PLL_IN_8M_OUT_120M PLL_NOT_SUPPORTED
#define PLL_IN_8M_OUT_128M 0x0120
/* PLL setting for 12M input clock */

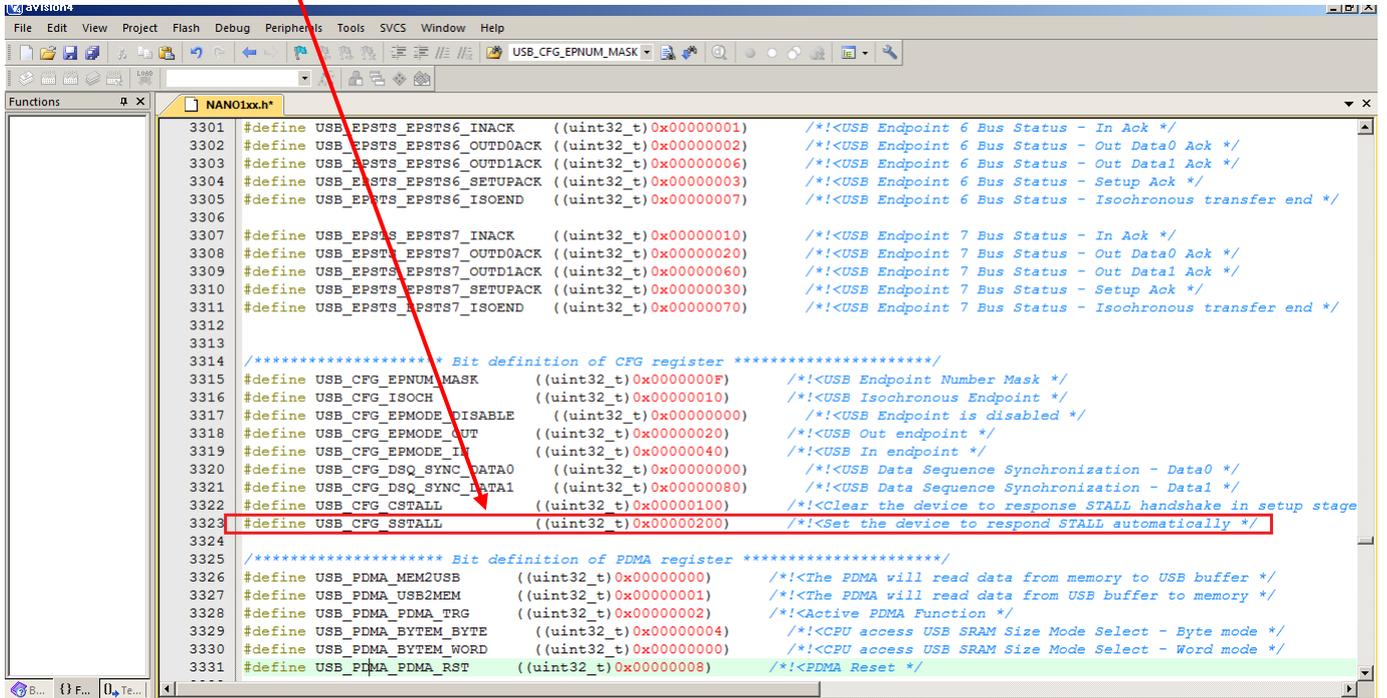
```

```
#define PLL_IN_12M_OUT_42M      0x0318
#define PLL_IN_12M_OUT_42M      0x0318
#define PLL_IN_12M_OUT_45M      PLL_NOT_SUPPORTED
#define PLL_IN_12M_OUT_48M      0x0320
#define PLL_IN_12M_OUT_84M      0x0218
#define PLL_IN_12M_OUT_90M      PLL_NOT_SUPPORTED
#define PLL_IN_12M_OUT_96M      0x0220
#define PLL_IN_12M_OUT_120M     0x0108
#define PLL_IN_12M_OUT_128M     PLL_NOT_SUPPORTED
/* PLL setting for 16M input clock */
#define PLL_IN_16M_OUT_42M      0x030A
#define PLL_IN_16M_OUT_45M      PLL_NOT_SUPPORTED
#define PLL_IN_16M_OUT_48M      0x0310
#define PLL_IN_16M_OUT_84M      0x020A
#define PLL_IN_16M_OUT_90M      PLL_NOT_SUPPORTED
#define PLL_IN_16M_OUT_96M      0x0210
#define PLL_IN_16M_OUT_120M     PLL_NOT_SUPPORTED
#define PLL_IN_16M_OUT_128M     0x0220
/* PLL setting for 24M input clock */
#define PLL_IN_24M_OUT_42M      PLL_NOT_SUPPORTED
#define PLL_IN_24M_OUT_45M      PLL_NOT_SUPPORTED
#define PLL_IN_24M_OUT_48M      0x0300
#define PLL_IN_24M_OUT_84M      PLL_NOT_SUPPORTED
#define PLL_IN_24M_OUT_90M      PLL_NOT_SUPPORTED
#define PLL_IN_24M_OUT_96M      0x0200
#define PLL_IN_24M_OUT_120M     0x0208
#define PLL_IN_24M_OUT_128M     PLL_NOT_SUPPORTED
```

Thêm dòng

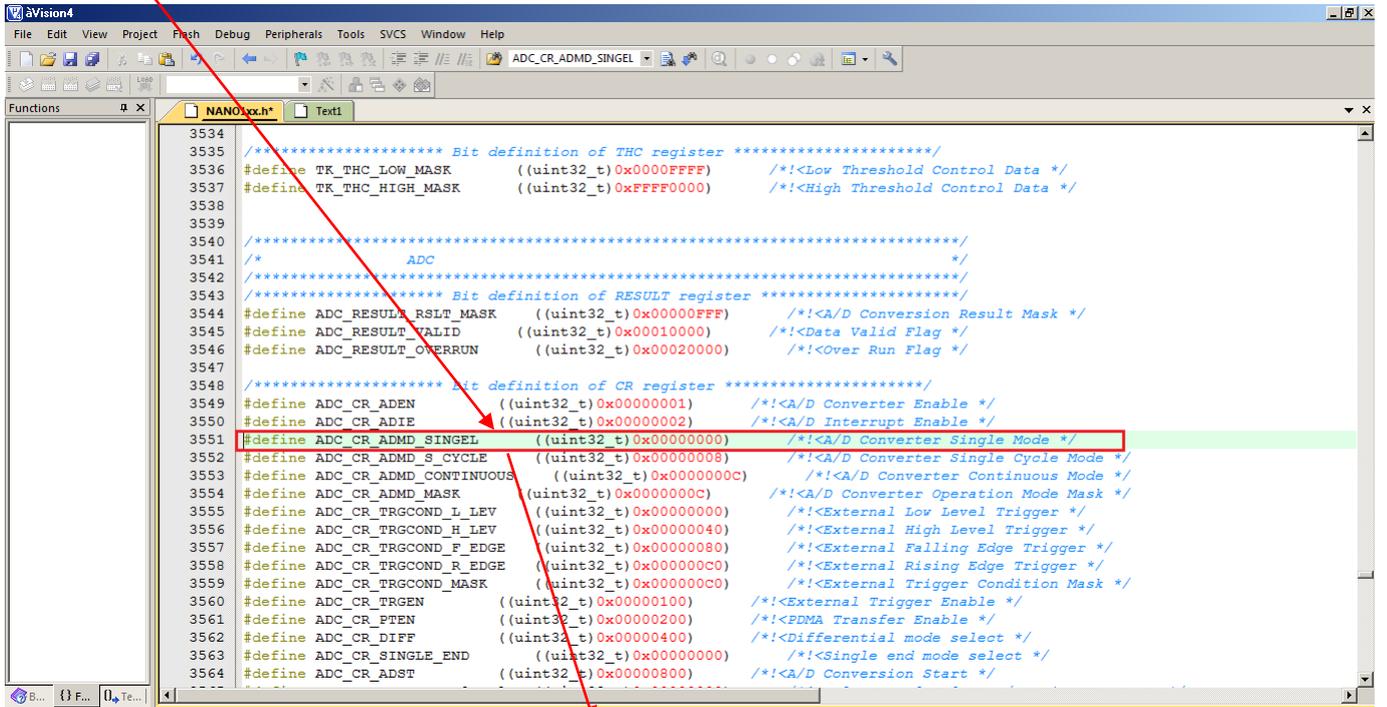
```
#define USB_CFG_CLRRDY ((uint32_t)0x00008000) /*!<Clear Ready */
```

Vào sau dòng dòng này



```
3301 #define USB_EPSTS_EPSTS6_INACK ((uint32_t)0x00000001) /*!<USB Endpoint 6 Bus Status - In Ack */
3302 #define USB_EPSTS_EPSTS6_OUTD0ACK ((uint32_t)0x00000002) /*!<USB Endpoint 6 Bus Status - Out Data0 Ack */
3303 #define USB_EPSTS_EPSTS6_OUTD1ACK ((uint32_t)0x00000006) /*!<USB Endpoint 6 Bus Status - Out Data1 Ack */
3304 #define USB_EPSTS_EPSTS6_SETUPACK ((uint32_t)0x00000003) /*!<USB Endpoint 6 Bus Status - Setup Ack */
3305 #define USB_EPSTS_EPSTS6_ISOEND ((uint32_t)0x00000007) /*!<USB Endpoint 6 Bus Status - Isochronous transfer end */
3306
3307 #define USB_EPSTS_EPSTS7_INACK ((uint32_t)0x00000010) /*!<USB Endpoint 7 Bus Status - In Ack */
3308 #define USB_EPSTS_EPSTS7_OUTD0ACK ((uint32_t)0x00000020) /*!<USB Endpoint 7 Bus Status - Out Data0 Ack */
3309 #define USB_EPSTS_EPSTS7_OUTD1ACK ((uint32_t)0x00000060) /*!<USB Endpoint 7 Bus Status - Out Data1 Ack */
3310 #define USB_EPSTS_EPSTS7_SETUPACK ((uint32_t)0x00000030) /*!<USB Endpoint 7 Bus Status - Setup Ack */
3311 #define USB_EPSTS_EPSTS7_ISOEND ((uint32_t)0x00000070) /*!<USB Endpoint 7 Bus Status - Isochronous transfer end */
3312
3313
3314 /****** Bit definition of CFG register *****/
3315 #define USB_CFG_EPNUM_MASK ((uint32_t)0x0000000F) /*!<USB Endpoint Number Mask */
3316 #define USB_CFG_ISOCH ((uint32_t)0x00000010) /*!<USB Isochronous Endpoint */
3317 #define USB_CFG_EPMODE_DISABLE ((uint32_t)0x00000000) /*!<USB Endpoint is disabled */
3318 #define USB_CFG_EPMODE_OUT ((uint32_t)0x00000020) /*!<USB Out endpoint */
3319 #define USB_CFG_EPMODE_IN ((uint32_t)0x00000040) /*!<USB In endpoint */
3320 #define USB_CFG_DSQ_SYNC_DATA0 ((uint32_t)0x00000000) /*!<USB Data Sequence Synchronization - Data0 */
3321 #define USB_CFG_DSQ_SYNC_DATA1 ((uint32_t)0x00000080) /*!<USB Data Sequence Synchronization - Data1 */
3322 #define USB_CFG_CSTALL ((uint32_t)0x00000100) /*!<Clear the device to response STALL handshake in setup stage */
3323 #define USB_CFG_SSTALL ((uint32_t)0x00000200) /*!<Set the device to respond STALL automatically */
3324
3325 /****** Bit definition of PDMA register *****/
3326 #define USB_PDMA_MEM2USB ((uint32_t)0x00000000) /*!<The PDMA will read data from memory to USB buffer */
3327 #define USB_PDMA_USB2MEM ((uint32_t)0x00000001) /*!<The PDMA will read data from USB buffer to memory */
3328 #define USB_PDMA_PDMA_TRG ((uint32_t)0x00000002) /*!<Active PDMA Function */
3329 #define USB_PDMA_BYTEM_BYTE ((uint32_t)0x00000004) /*!<CPU access USB SRAM Size Mode Select - Byte mode */
3330 #define USB_PDMA_BYTEM_WORD ((uint32_t)0x00000000) /*!<CPU access USB SRAM Size Mode Select - Word mode */
3331 #define USB_PDMA_RST ((uint32_t)0x00000008) /*!<PDMA Reset */
```

Sửa dòng



```

3534
3535 /****** Bit definition of THCR register *****/
3536 #define TK_THC_LOW_MASK ((uint32_t)0x0000FFFF) /*!<Low Threshold Control Data */
3537 #define TK_THC_HIGH_MASK ((uint32_t)0xFFFF0000) /*!<High Threshold Control Data */
3538
3539
3540 /****** Bit definition of ADC register *****/
3541 /*
3542 ADC
3543 *****/
3544 /****** Bit definition of RESULT register *****/
3545 #define ADC_RESULT_RSLT_MASK ((uint32_t)0x000000FF) /*!<A/D Conversion Result Mask */
3546 #define ADC_RESULT_VALID ((uint32_t)0x00010000) /*!<Data Valid Flag */
3547 #define ADC_RESULT_OVERRUN ((uint32_t)0x00020000) /*!<Over Run Flag */
3548
3549 /****** Bit definition of CR register *****/
3550 #define ADC_CR_ADEN ((uint32_t)0x00000001) /*!<A/D Converter Enable */
3551 #define ADC_CR_ADIE ((uint32_t)0x00000002) /*!<A/D Interrupt Enable */
3552 #define ADC_CR_ADMD_SINGEL ((uint32_t)0x00000000) /*!<A/D Converter Single Mode */
3553 #define ADC_CR_ADMD_S_CYCLE ((uint32_t)0x00000008) /*!<A/D Converter Single Cycle Mode */
3554 #define ADC_CR_ADMD_CONTINUOUS ((uint32_t)0x0000000C) /*!<A/D Converter Continuous Mode */
3555 #define ADC_CR_ADMD_MASK ((uint32_t)0x0000000C) /*!<A/D Converter Operation Mode Mask */
3556 #define ADC_CR_TRGCOND_L_LEV ((uint32_t)0x00000000) /*!<External Low Level Trigger */
3557 #define ADC_CR_TRGCOND_H_LEV ((uint32_t)0x00000040) /*!<External High Level Trigger */
3558 #define ADC_CR_TRGCOND_F_EDGE ((uint32_t)0x00000080) /*!<External Falling Edge Trigger */
3559 #define ADC_CR_TRGCOND_R_EDGE ((uint32_t)0x000000C0) /*!<External Rising Edge Trigger */
3560 #define ADC_CR_TRGCOND_MASK ((uint32_t)0x000000C0) /*!<External Trigger Condition Mask */
3561 #define ADC_CR_TRGEN ((uint32_t)0x00000100) /*!<External Trigger Enable */
3562 #define ADC_CR_PTEN ((uint32_t)0x00000200) /*!<PDMA Transfer Enable */
3563 #define ADC_CR_DIFF ((uint32_t)0x00000400) /*!<Differential mode select */
3564 #define ADC_CR_SINGLE_END ((uint32_t)0x00000800) /*!<Single end mode select */
3565 #define ADC_CR_ADST ((uint32_t)0x00000800) /*!<A/D Conversion Start */

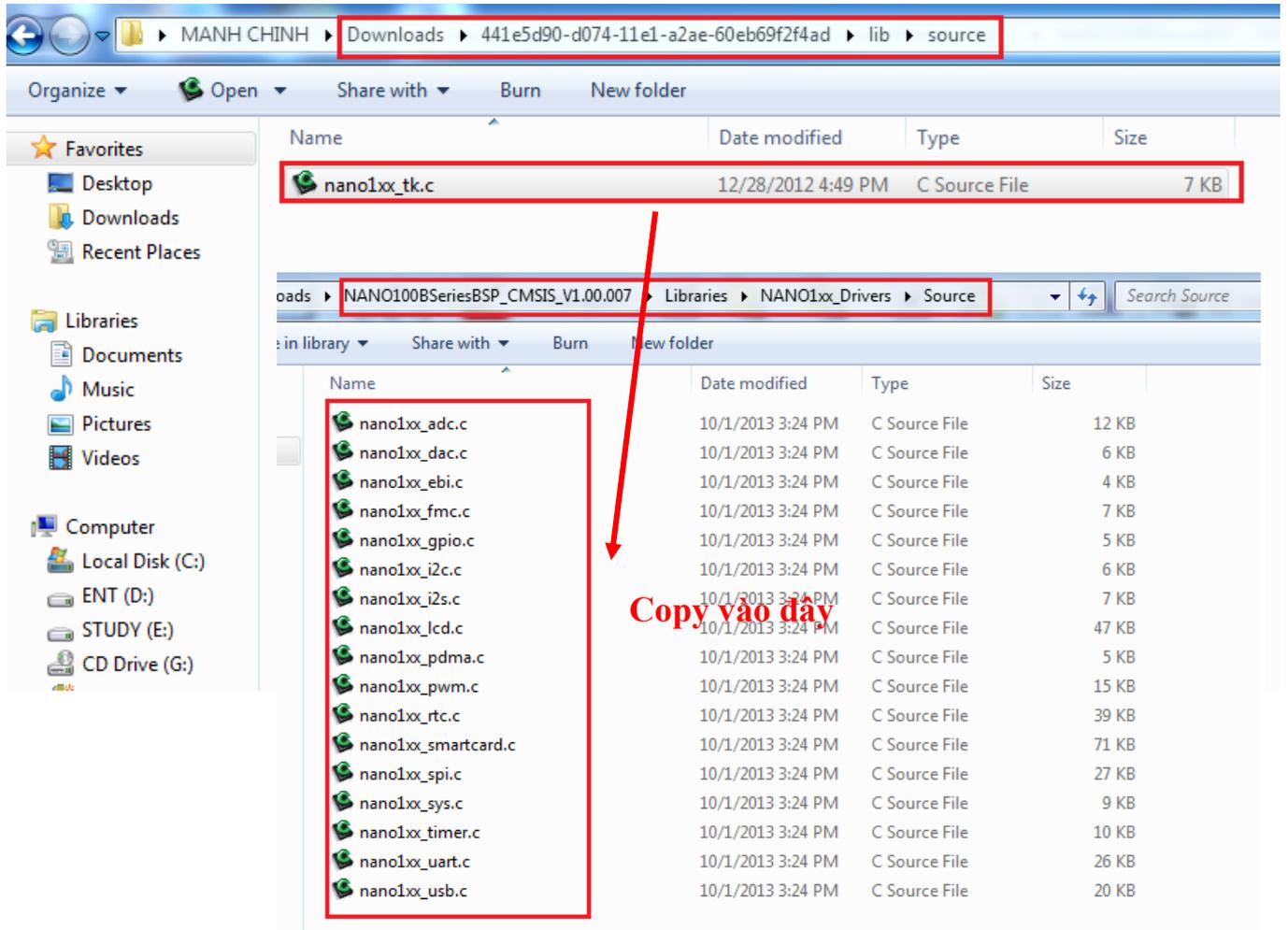
```

```
#define ADC_CR_ADMD_SINGEL ((uint32_t)0x00000000) /*!<A/D Converter Single Mode */
```

Bước 4: Thêm file thư viện Touch Key

Copy file [nano1xx\\_tk.c](#) tải ở trên vào thư mục:

[\\NANO100BSeriesBSP\CMSIS\\_V1.00.007\Libraries\NANO1xx\\_Drivers\Source](\\NANO100BSeriesBSP\CMSIS_V1.00.007\Libraries\NANO1xx_Drivers\Source)

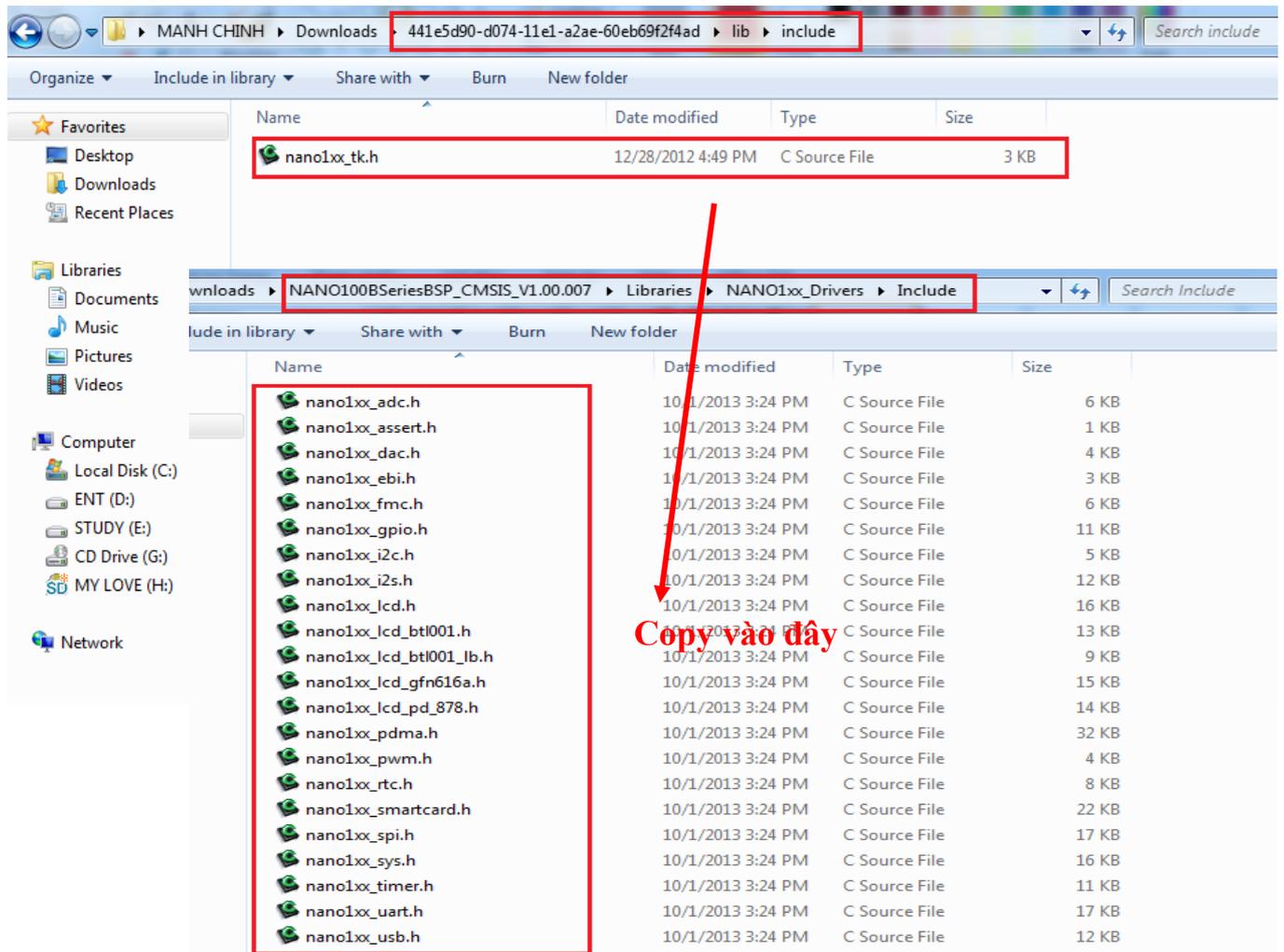


The screenshot displays two Windows Explorer windows. The top window shows the file 'nano1xx\_tk.c' (7 KB) in the 'Downloads' folder. The bottom window shows the target directory 'Source' containing various source files. A red arrow points from the file in the top window to the target directory in the bottom window, with the text 'Copy vào đây' (Copy here) written in red.

Name	Date modified	Type	Size
nano1xx_adc.c	10/1/2013 3:24 PM	C Source File	12 KB
nano1xx_dac.c	10/1/2013 3:24 PM	C Source File	6 KB
nano1xx_ebi.c	10/1/2013 3:24 PM	C Source File	4 KB
nano1xx_fmc.c	10/1/2013 3:24 PM	C Source File	7 KB
nano1xx_gpio.c	10/1/2013 3:24 PM	C Source File	5 KB
nano1xx_i2c.c	10/1/2013 3:24 PM	C Source File	6 KB
nano1xx_i2s.c	10/1/2013 3:24 PM	C Source File	7 KB
nano1xx_lcd.c	10/1/2013 3:24 PM	C Source File	47 KB
nano1xx_pdma.c	10/1/2013 3:24 PM	C Source File	5 KB
nano1xx_pwm.c	10/1/2013 3:24 PM	C Source File	15 KB
nano1xx_rtc.c	10/1/2013 3:24 PM	C Source File	39 KB
nano1xx_smartcard.c	10/1/2013 3:24 PM	C Source File	71 KB
nano1xx_spi.c	10/1/2013 3:24 PM	C Source File	27 KB
nano1xx_sys.c	10/1/2013 3:24 PM	C Source File	9 KB
nano1xx_timer.c	10/1/2013 3:24 PM	C Source File	10 KB
nano1xx_uart.c	10/1/2013 3:24 PM	C Source File	26 KB
nano1xx_usb.c	10/1/2013 3:24 PM	C Source File	20 KB

Copy file [nano1xx\\_tk.c](#) tải ở trên vào thư mục:

\\NANO100BSeriesBSP\CMSIS\_V1.00.007\Libraries\NANO1xx\_Drivers\Include



The screenshot shows two windows of Windows Explorer. The top window shows the path: MANH CHINH > Downloads > 441e5d90-d074-11e1-a2ae-60eb69f2f4ad > lib > include. A file named 'nano1xx\_tk.h' is highlighted in the list. The bottom window shows the path: Downloads > NANO100BSeriesBSP\CMSIS\_V1.00.007 > Libraries > NANO1xx\_Drivers > Include. A list of source files is shown, with a red box around the entire list and a red arrow pointing to it from the text 'Copy vào đây'.

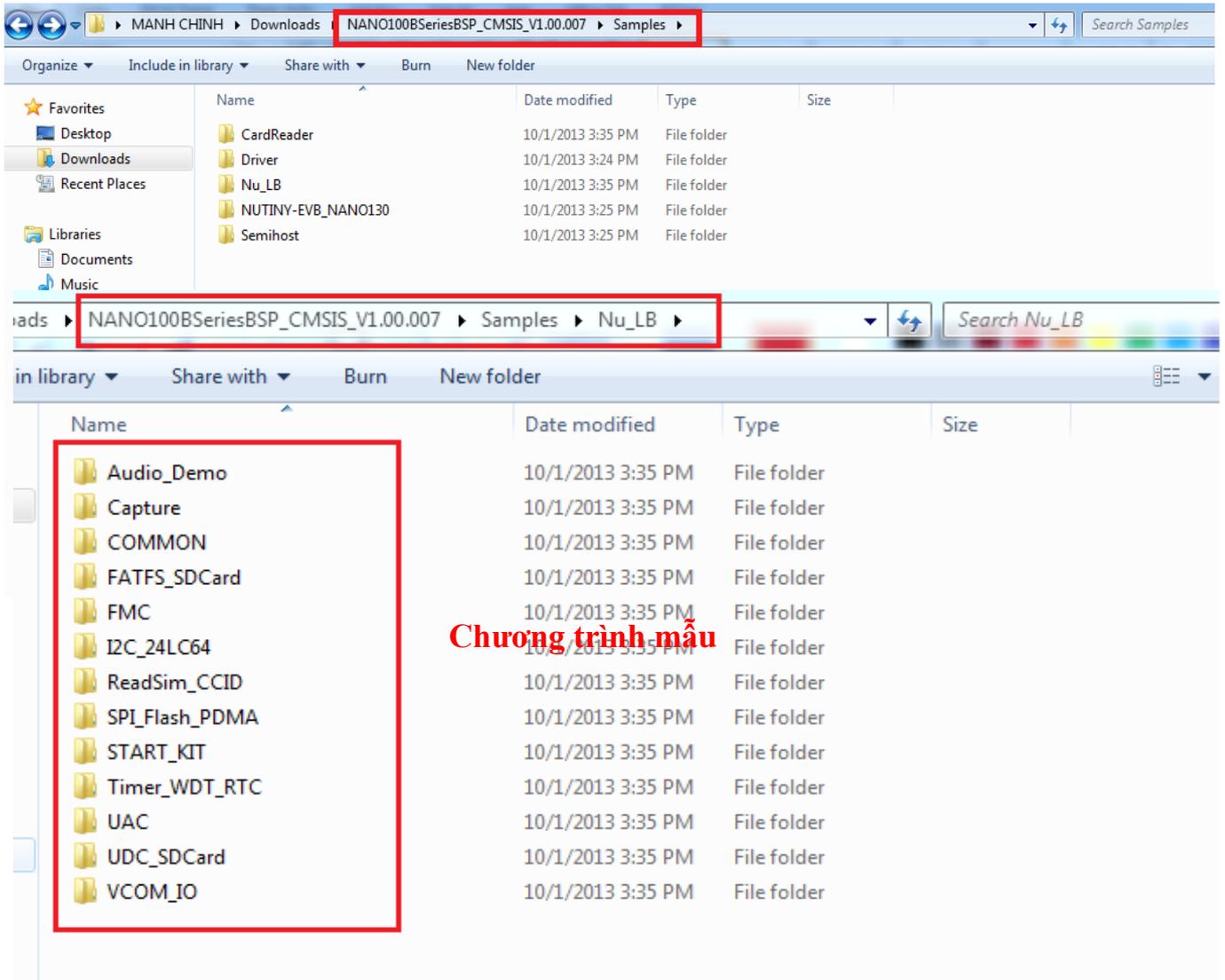
Name	Date modified	Type	Size
nano1xx_adc.h	10/1/2013 3:24 PM	C Source File	6 KB
nano1xx_assert.h	10/1/2013 3:24 PM	C Source File	1 KB
nano1xx_dac.h	10/1/2013 3:24 PM	C Source File	4 KB
nano1xx_ebi.h	10/1/2013 3:24 PM	C Source File	3 KB
nano1xx_fmcc.h	10/1/2013 3:24 PM	C Source File	6 KB
nano1xx_gpio.h	10/1/2013 3:24 PM	C Source File	11 KB
nano1xx_i2c.h	10/1/2013 3:24 PM	C Source File	5 KB
nano1xx_i2s.h	10/1/2013 3:24 PM	C Source File	12 KB
nano1xx_lcd.h	10/1/2013 3:24 PM	C Source File	16 KB
nano1xx_lcd_bt1001.h	10/1/2013 3:24 PM	C Source File	13 KB
nano1xx_lcd_bt1001_lb.h	10/1/2013 3:24 PM	C Source File	9 KB
nano1xx_lcd_gfn616a.h	10/1/2013 3:24 PM	C Source File	15 KB
nano1xx_lcd_pd_878.h	10/1/2013 3:24 PM	C Source File	14 KB
nano1xx_pdma.h	10/1/2013 3:24 PM	C Source File	32 KB
nano1xx_pwm.h	10/1/2013 3:24 PM	C Source File	4 KB
nano1xx_rtc.h	10/1/2013 3:24 PM	C Source File	8 KB
nano1xx_smartcard.h	10/1/2013 3:24 PM	C Source File	22 KB
nano1xx_spi.h	10/1/2013 3:24 PM	C Source File	17 KB
nano1xx_sys.h	10/1/2013 3:24 PM	C Source File	16 KB
nano1xx_timer.h	10/1/2013 3:24 PM	C Source File	11 KB
nano1xx_uart.h	10/1/2013 3:24 PM	C Source File	17 KB
nano1xx_usb.h	10/1/2013 3:24 PM	C Source File	12 KB

### 7. Lập trình Nano100 Series

Trong phần này sẽ hướng dẫn lập trình trên KeilC

Cũng giống như các dòng vi điều khiển khác của Nuvoton như NUC100 Series, M051, Mini51... hay như các dòng ARM khác, cách thức tạo Project cho những ứng dụng sử dụng dòng Nano100 Series cũng tương tự. Bạn có thể tham khảo tại đây:

[http://tula.vn/modules.php?name=monline&file=sdtdc1&\\_run=view&cid=84&arrange=tu5&desc=1&showcol=52735&showtype=0](http://tula.vn/modules.php?name=monline&file=sdtdc1&_run=view&cid=84&arrange=tu5&desc=1&showcol=52735&showtype=0)



Name	Date modified	Type	Size
CardReader	10/1/2013 3:35 PM	File folder	
Driver	10/1/2013 3:24 PM	File folder	
Nu_LB	10/1/2013 3:35 PM	File folder	
NUTINY-EVB_NANO130	10/1/2013 3:25 PM	File folder	
Semihost	10/1/2013 3:25 PM	File folder	

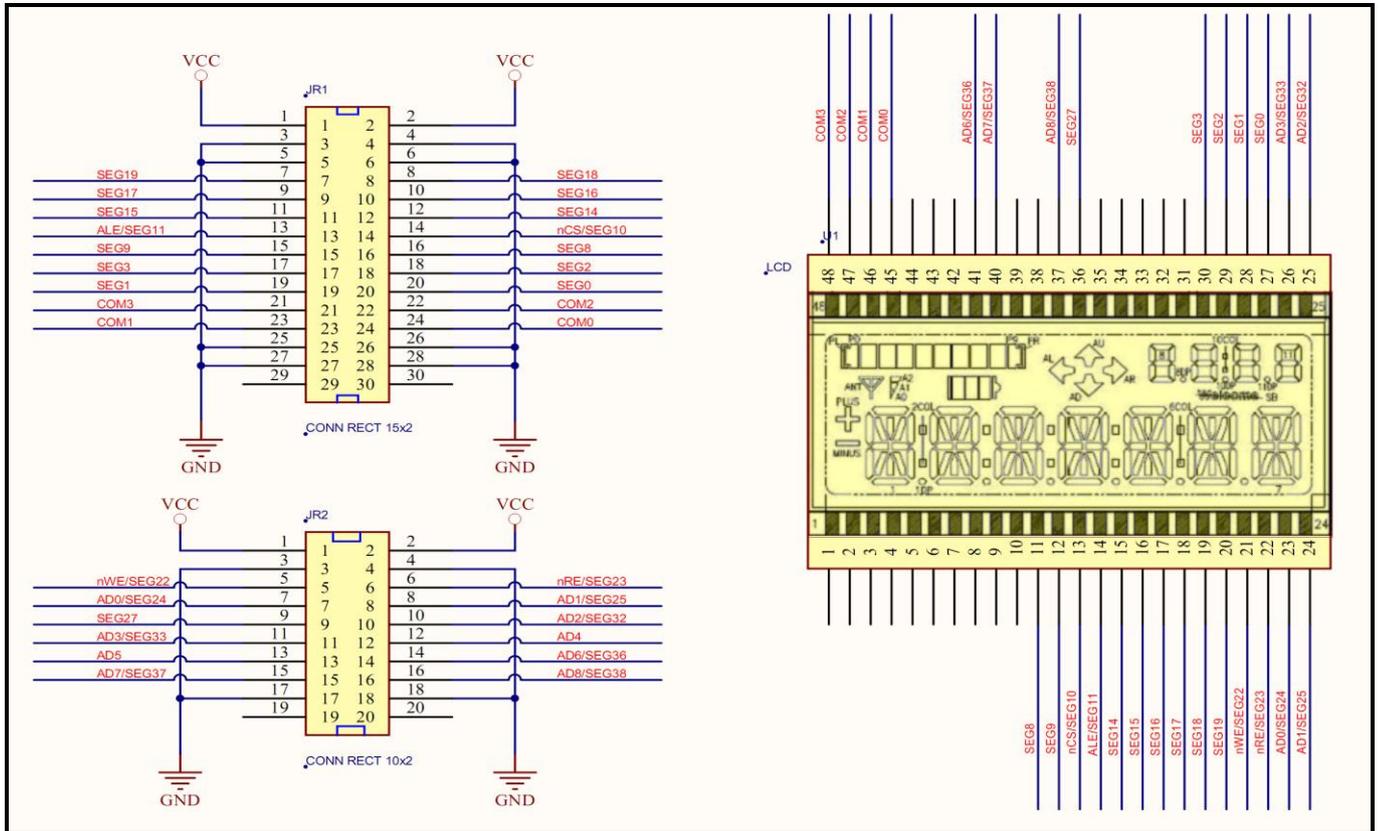
  

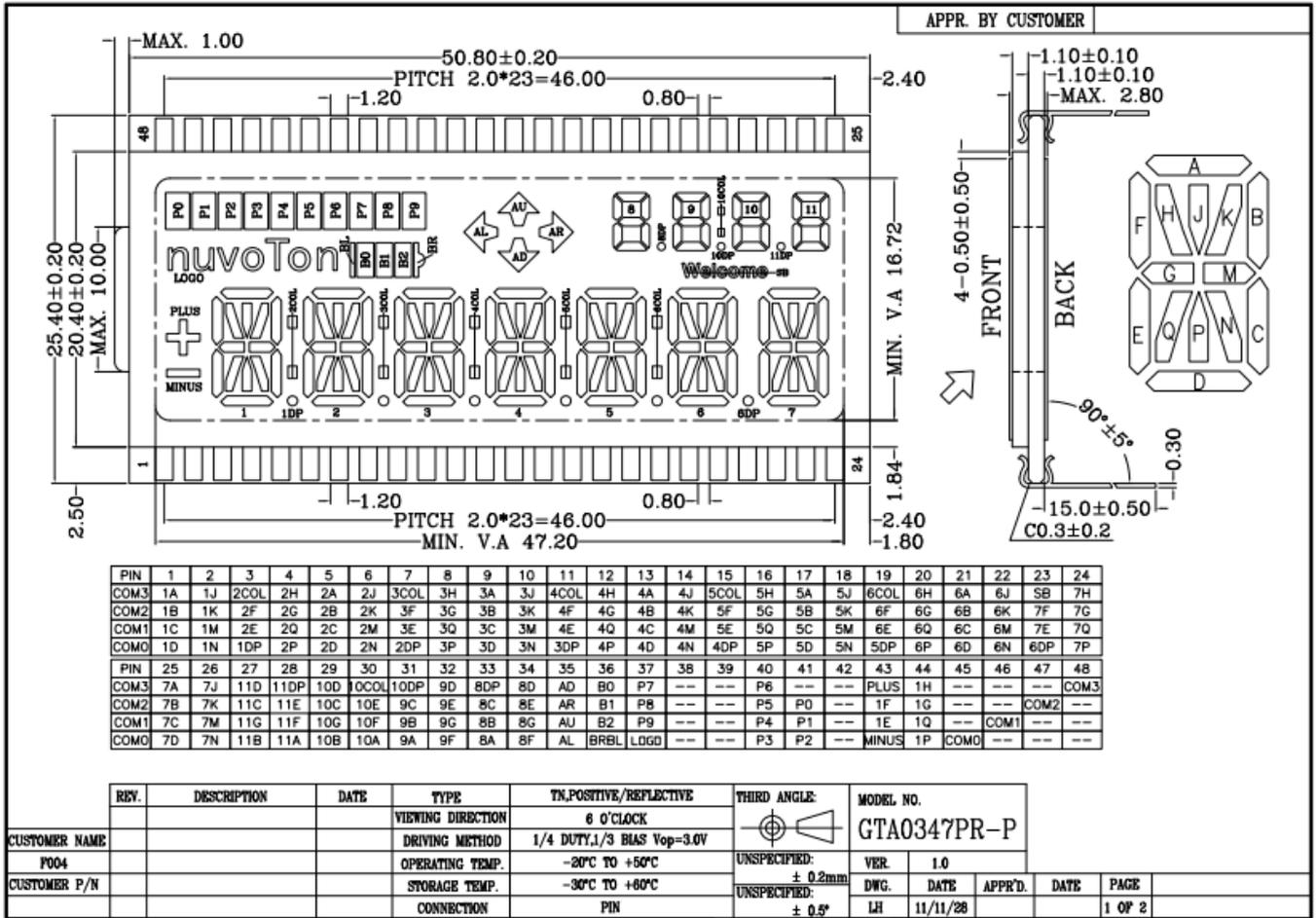
Name	Date modified	Type	Size
Audio_Demo	10/1/2013 3:35 PM	File folder	
Capture	10/1/2013 3:35 PM	File folder	
COMMON	10/1/2013 3:35 PM	File folder	
FATFS_SDCard	10/1/2013 3:35 PM	File folder	
FMC	10/1/2013 3:35 PM	File folder	
I2C_24LC64	10/1/2013 3:35 PM	File folder	
ReadSim_CCID	10/1/2013 3:35 PM	File folder	
SPI_Flash_PDMA	10/1/2013 3:35 PM	File folder	
START_KIT	10/1/2013 3:35 PM	File folder	
Timer_WDT_RTC	10/1/2013 3:35 PM	File folder	
UAC	10/1/2013 3:35 PM	File folder	
UDC_SDCard	10/1/2013 3:35 PM	File folder	
VCOM_IO	10/1/2013 3:35 PM	File folder	

**Chương trình mẫu**

**7.1 Giao tiếp LCD**

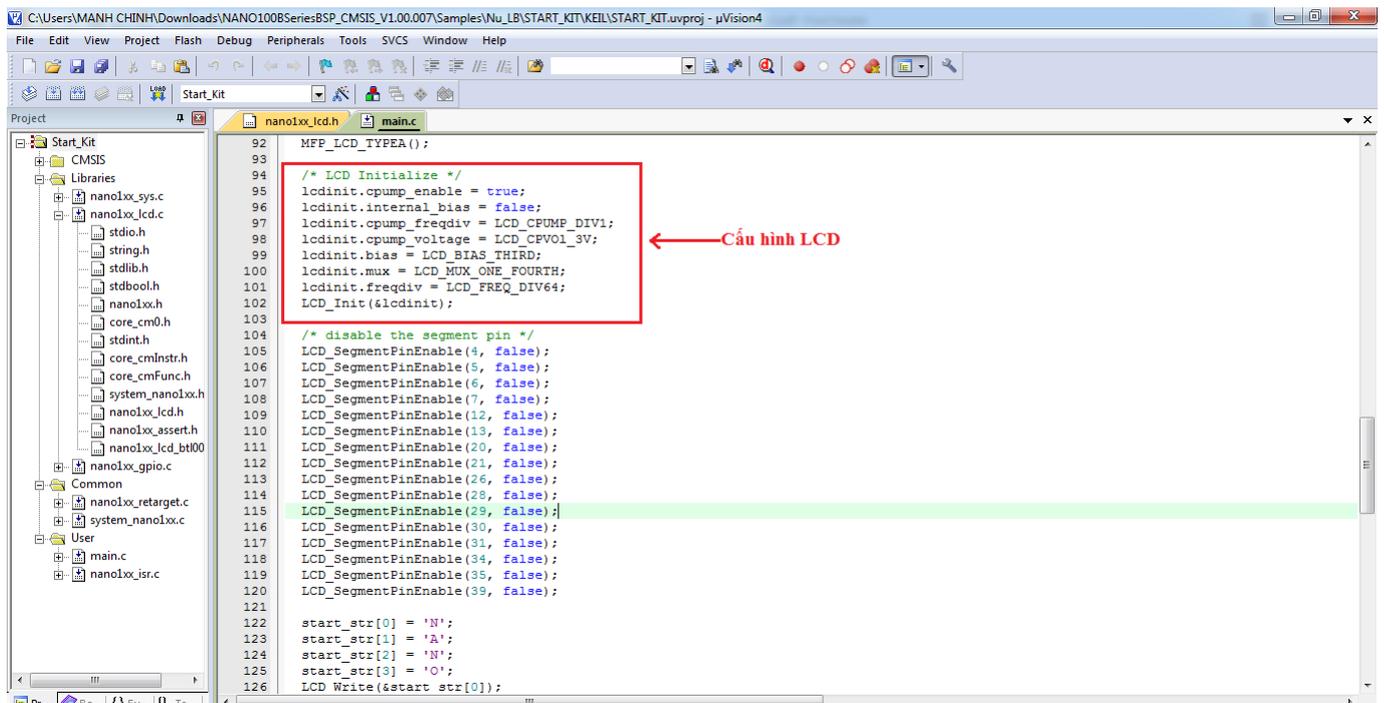
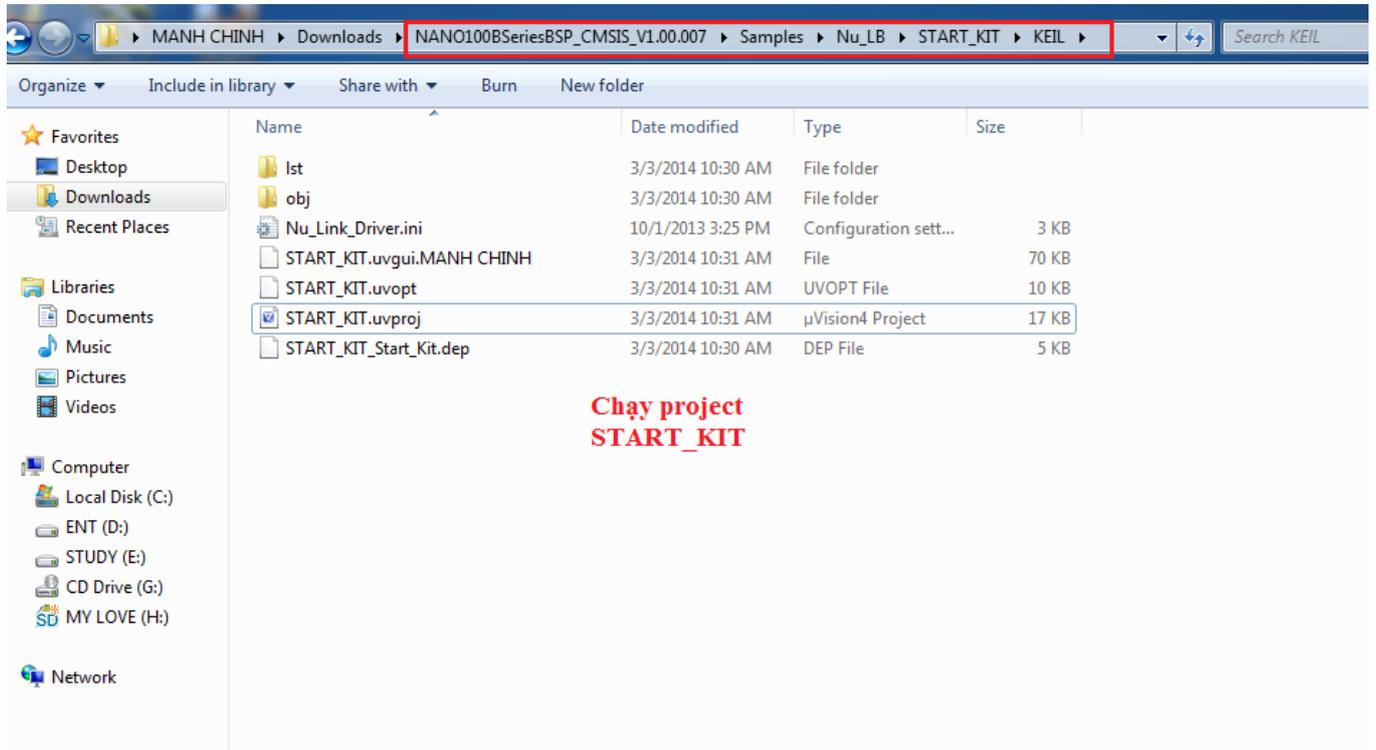
**a) Mạch nguyên lý**

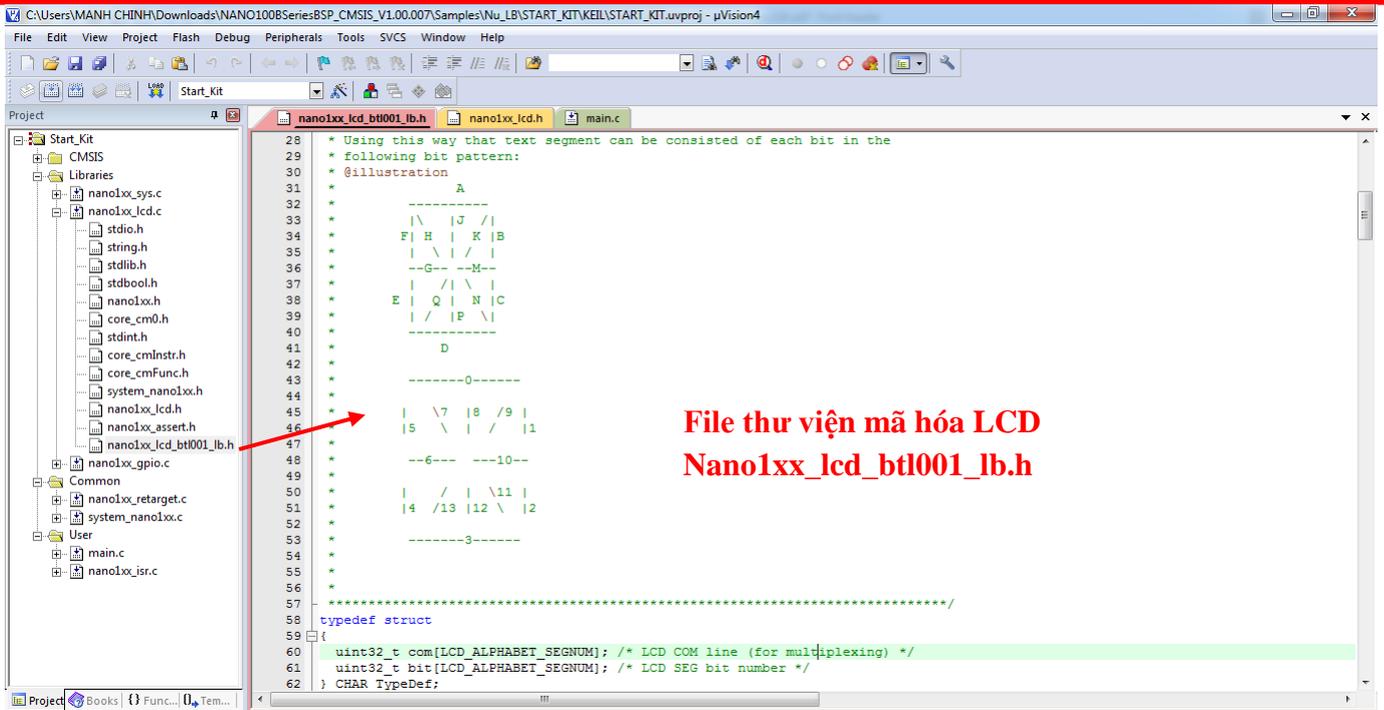




GLCD GTA0347PR

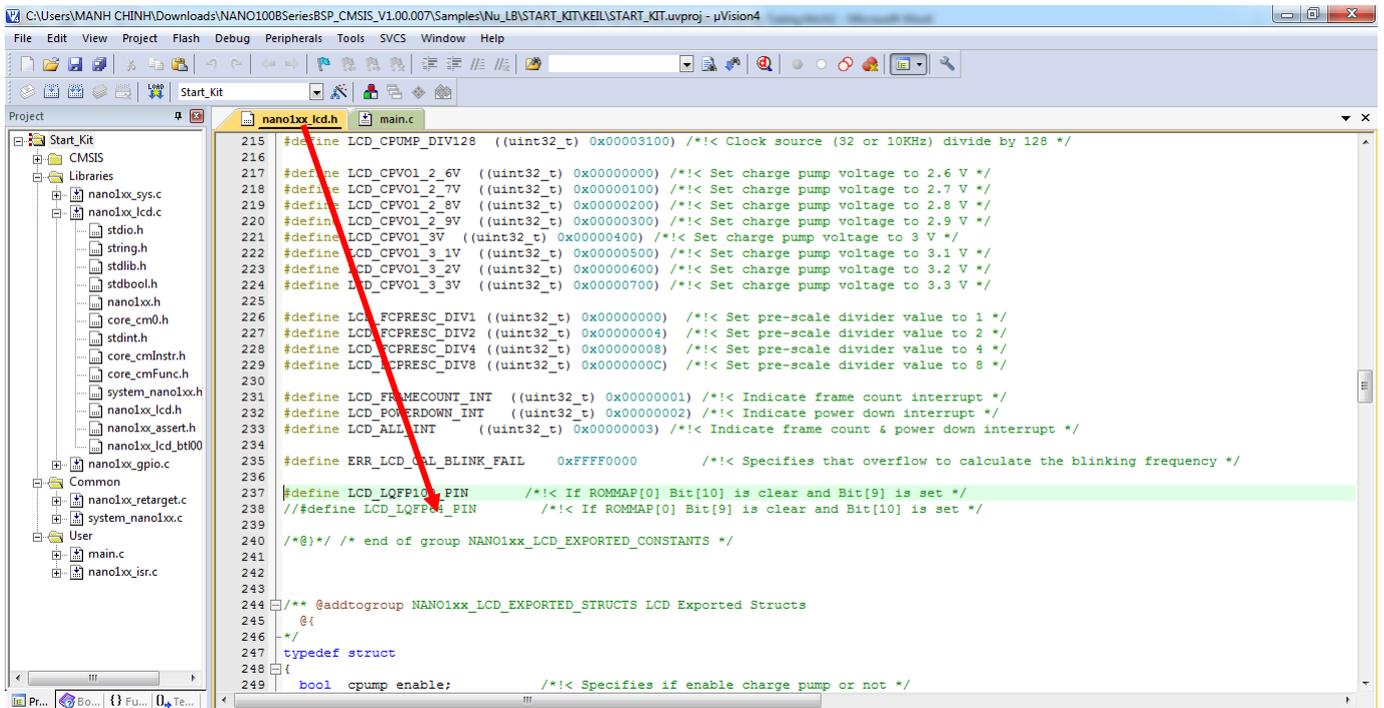
## b) Code mẫu





### Lưu ý:

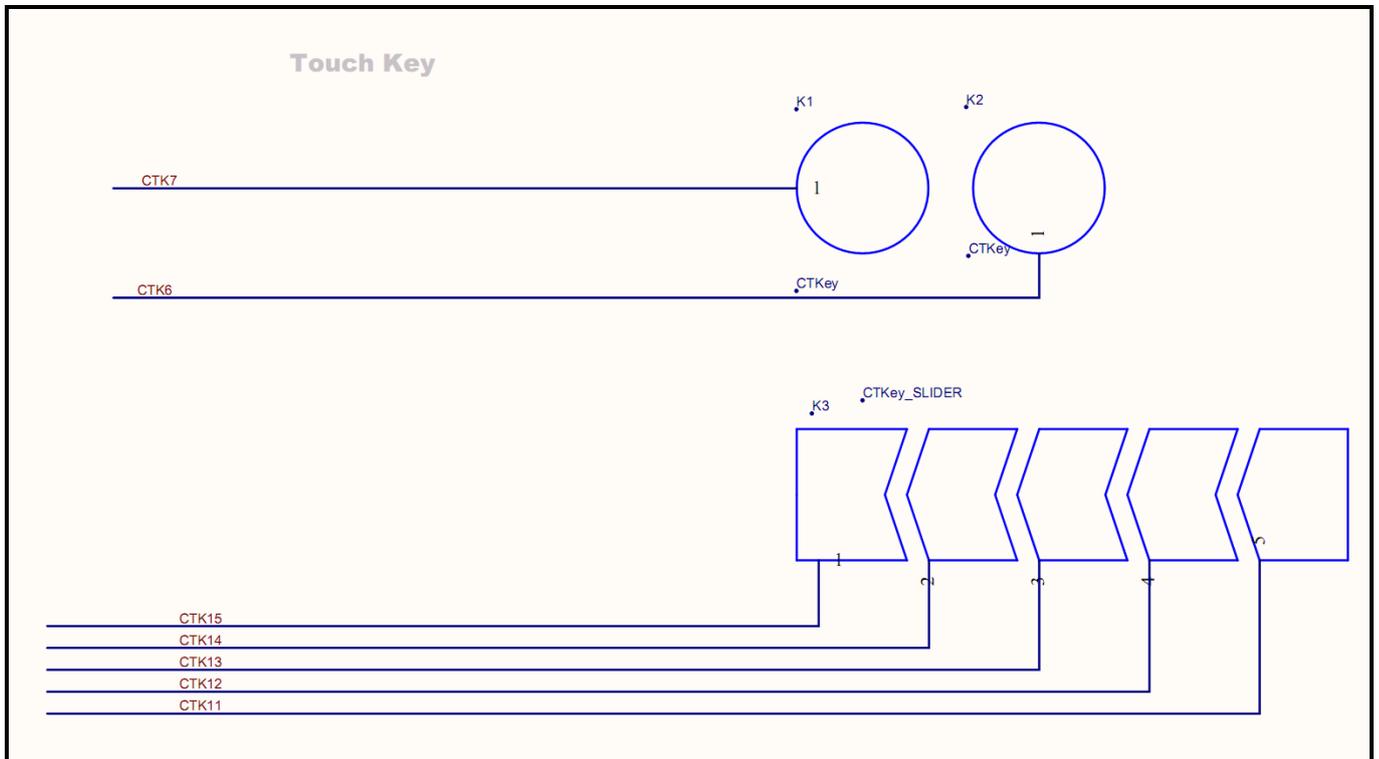
Đồng Nano100 Series(Có hỗ trợ giao tiếp LCD) gồm 2 loại: 64 chân và 128 chân. Lựa chọn loại phù hợp trong khi viết các ứng dụng



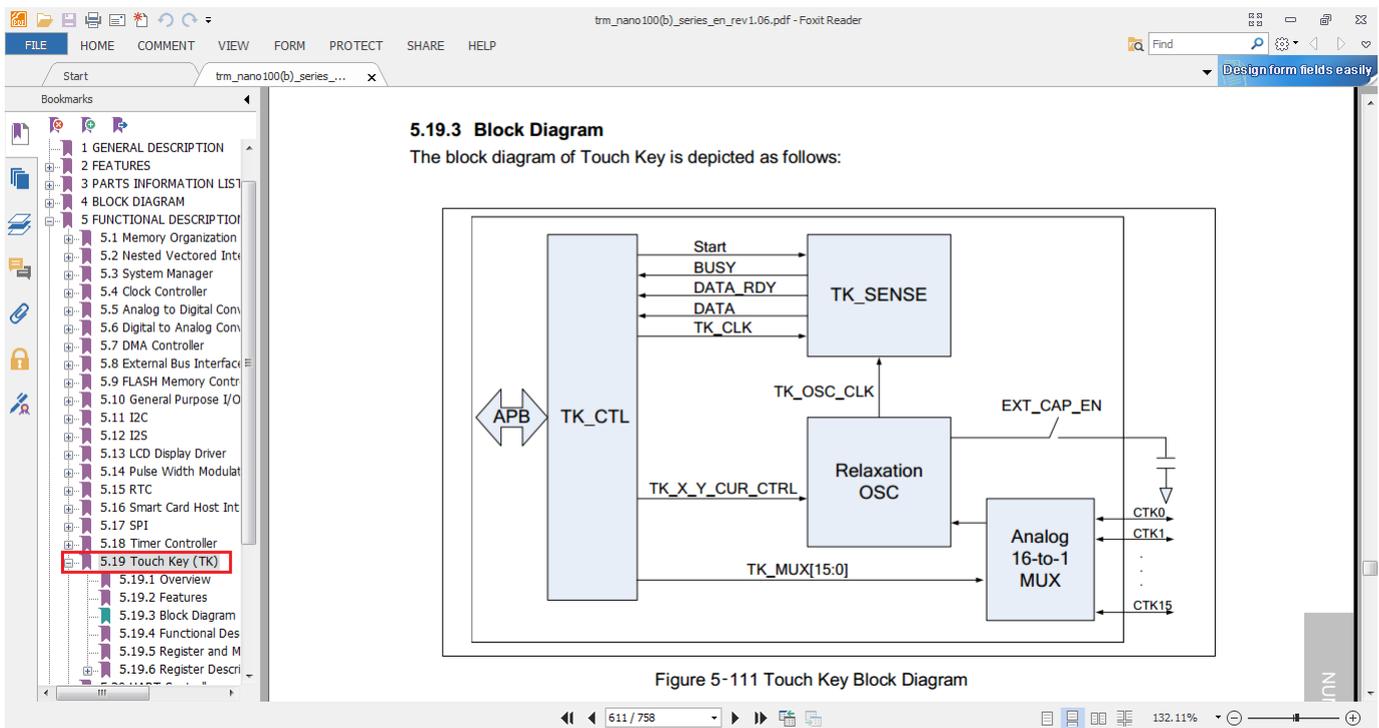
Biên dịch chương trình, nạp xuống Kit Nu\_LB-Nano130 và xem kết quả.

## 7.2 Giao tiếp Touch Key

### a) Mạch nguyên lý



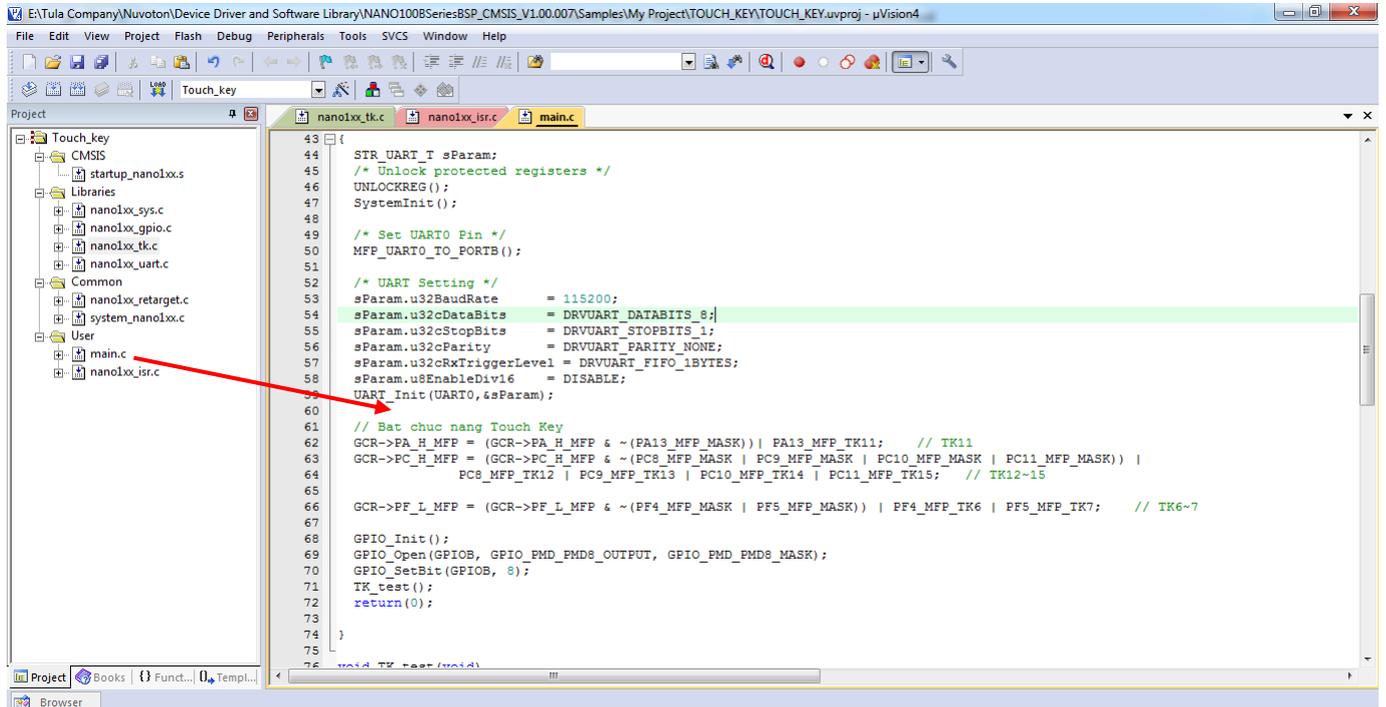
Chi tiết về giao tiếp Touch key ở đây



## b) Code mẫu

Khi chạm K1 hoặc K2 thì led sáng

### File main.c



```

43 {
44     STR_UART_T sParam;
45     /* Unlock protected registers */
46     UNLOCKREG();
47     SystemInit();
48
49     /* Set UART0 Pin */
50     MFP_UART0_TO_PORTB();
51
52     /* UART Setting */
53     sParam.u32BaudRate      = 115200;
54     sParam.u32cDataBits     = DRVUART_DATABITS_8;
55     sParam.u32cStopBits     = DRVUART_STOPBITS_1;
56     sParam.u32cParity       = DRVUART_PARITY_NONE;
57     sParam.u32cRxTriggerLevel = DRVUART_FIFO_1BYTES;
58     sParam.u8EnableDiv16    = DISABLE;
59     UART_Init(UART0, &sParam);
60
61     // Bat chuc nang Touch Key
62     GCR->PA_H_MFP = (GCR->PA_H_MFP & ~(PA13_MFP_MASK)) | PA13_MFP_TK11; // TK11
63     GCR->PC_H_MFP = (GCR->PC_H_MFP & ~(PC8_MFP_MASK | PC9_MFP_MASK | PC10_MFP_MASK | PC11_MFP_MASK)) |
64     PC8_MFP_TK12 | PC9_MFP_TK13 | PC10_MFP_TK14 | PC11_MFP_TK15; // TK12-15
65
66     GCR->PF_L_MFP = (GCR->PF_L_MFP & ~(PF4_MFP_MASK | PF5_MFP_MASK)) | PF4_MFP_TK6 | PF5_MFP_TK7; // TK6-7
67
68     GPIO_Init();
69     GPIO_Open(GPIOB, GPIO_FMD_FMD8_OUTPUT, GPIO_FMD_FMD8_MASK);
70     GPIO_SetBit(GPIOB, 8);
71     TK_test();
72     return(0);
73 }
74
75
76 void TK_test(void)

```

### Code chương trình:

```

#include <stdio.h>
#include "nanolxx_sys.h"
#include "nanolxx_lcd.h"
#include "nanolxx_gpio.h"
#include "nanolxx_uart.h"
#include "nanolxx_tk.h"

#define TK_HIGH_THRESHOLD      0x0000
#define TK_LOW_THRESHOLD      0xFFFF
#define TK_DATA_THRESHOLD     0xA100

void TK_test(void);

uint8_t fail, th;
uint16_t ch6_data, ch7_data;
uint8_t volatile complete = 0;

void delay_loop(void)
{
    __IO uint32_t i, j;

    for(i=0; i<3; i++)
    {
        for(j=0; j<60000; j++);
    }
}

```

```

    }
}

/**
 * @brief main function.
 * @param None
 * @return None
 */
int32_t main(void)
{
    STR_UART_T sParam;
    /* Unlock protected registers */
    UNLOCKREG();
    SystemInit();

    /* Set UART0 Pin */
    MFP_UART0_TO_PORTB();

    /* UART Setting */
    sParam.u32BaudRate           = 115200;
    sParam.u32cDataBits          = DRVUART_DATABITS_8;
    sParam.u32cStopBits          = DRVUART_STOPBITS_1;
    sParam.u32cParity             = DRVUART_PARITY_NONE;
    sParam.u32cRxTriggerLevel    = DRVUART_FIFO_1BYTES;
    sParam.u8EnableDiv16         = DISABLE;
    UART_Init(UART0, &sParam);

    // Bat chuc nang Touch Key
    GCR->PA_H_MFP = (GCR->PA_H_MFP & ~(PA13_MFP_MASK)) | PA13_MFP_TK11; // TK11
    GCR->PC_H_MFP = (GCR->PC_H_MFP & ~(PC8_MFP_MASK | PC9_MFP_MASK |
        PC10_MFP_MASK | PC11_MFP_MASK)) | PC8_MFP_TK12 | PC9_MFP_TK13 |
        PC10_MFP_TK14 | PC11_MFP_TK15; // TK12~15

    GCR->PF_L_MFP = (GCR->PF_L_MFP & ~(PF4_MFP_MASK | PF5_MFP_MASK)) |
        PF4_MFP_TK6 | PF5_MFP_TK7; // TK6~7

    GPIO_Init();
    GPIO_Open(GPIOB, GPIO_PMD_PMD8_OUTPUT, GPIO_PMD_PMD8_MASK);
    GPIO_SetBit(GPIOB, 8);
    TK_test();
    return(0);
}

void TK_test(void)
{
    uint32_t reg;
    uint8_t i;

    S_TK_CH_CFG ch_cfg;
    ch_cfg.u8Level = 8;

```



```
ch_cfg.u8Div = 2;
ch_cfg.ul6HighThld = TK_HIGH_THRESHOLD;
ch_cfg.ul6LowThld = TK_LOW_THRESHOLD;

TK_Init(TK_CTL1_SEN_SEL_16BIT); // Do nhay 16 bit
/* Cau hinh TK6, TK7*/
TK_ConfigChannel(6, &ch_cfg);
TK_ConfigChannel(7, &ch_cfg);

/* Cho phep ngat */
TK_EnableInterrupt(TK_INT_ALL);

printf("===== Nano 100 series touch key =====");
while(1)
{
    complete = 0;

    reg = TK_CTL1_EN_TK14_6 | TK_CTL1_EN_TK15_7; // Lua chon get canh 6 va 7
    TK->CTL1 = (TK->CTL1 & (0xffff<<16)) | reg | TK_CTL1_START_BY_SW;//bat
    dau quet

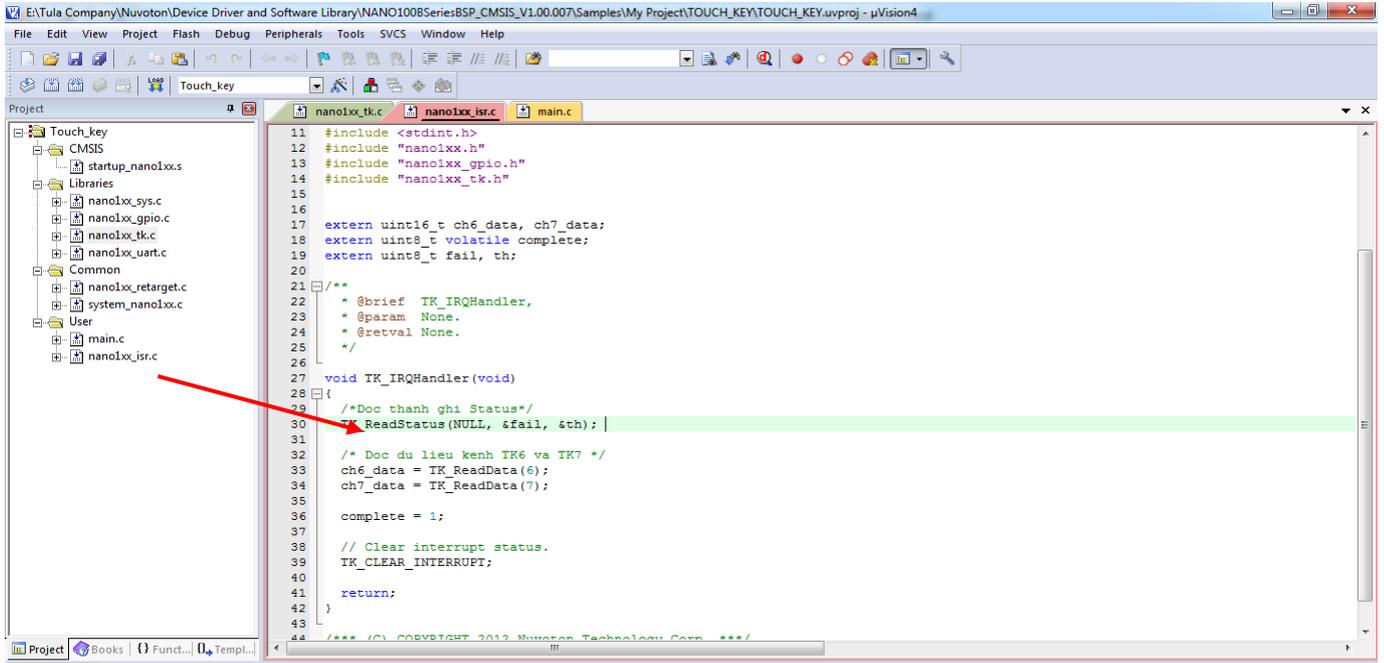
    while(complete == 0); // doi den khi chuyen doi xong

    printf("ch%02d: l_th-%04x h_th-%04x data-%04x %04x %04x\n\r",
           6, TK_LOW_THRESHOLD,TK_LOW_THRESHOLD,ch6_data,fail,th);
    printf("ch%02d: l_th-%04x h_th-%04x data-%04x %04x %04x\n\r",
           7, TK_LOW_THRESHOLD,TK_LOW_THRESHOLD,ch7_data,fail,th);
    /* Neu TK6 hoac TK7 lon hon TK_DATA_THRESHOLD thi sang led*/
    if((ch6_data>=TK_DATA_THRESHOLD)|| (ch7_data>=TK_DATA_THRESHOLD))
        GPIO_ClrBit(GPIOB, 8);
    else
        GPIO_SetBit(GPIOB, 8);

    for(i=0; i<5; i++)
        delay_loop();
}
return;
}

#ifdef USE_ASSERT
void assert_error(uint8_t * file, uint32_t line)
{
    printf("[%s] line %d : wrong parameters.\r\n", file, line);
    /* Infinite loop */
    while(1) ;
}
#endif
```

## File nano1xx\_isr.c



```
11 #include <stdint.h>
12 #include "nano1xx.h"
13 #include "nano1xx_gpio.h"
14 #include "nano1xx_tk.h"
15
16 extern uint16_t ch6_data, ch7_data;
17 extern uint8_t volatile complete;
18 extern uint8_t fail, th;
19
20 /**
21  * @brief TK_IRQHandler,
22  * @param None.
23  * @retval None.
24  */
25
26 void TK_IRQHandler(void)
27 {
28     /*Doc thanh ghi Status*/
29     TK_ReadStatus(NULL, &fail, &th);
30
31     /* Doc du lieu kenh TK6 va TK7 */
32     ch6_data = TK_ReadData(6);
33     ch7_data = TK_ReadData(7);
34
35     complete = 1;
36
37     // Clear interrupt status.
38     TK_CLEAR_INTERRUPT;
39
40     return;
41 }
42
43
44 /** (C) COPYRIGHT 2012 Nuvoton Technology Corp. **/
```

## Code chương trình

```
#include <stdint.h>
#include "nano1xx.h"
#include "nano1xx_gpio.h"
#include "nano1xx_tk.h"

extern uint16_t ch6_data, ch7_data;
extern uint8_t volatile complete;
extern uint8_t fail, th;

/**
 * @brief TK_IRQHandler,
 * @param None.
 * @retval None.
 */
void TK_IRQHandler(void)
{
    /*Doc thanh ghi Status*/
    TK_ReadStatus(NULL, &fail, &th);
    /* Doc du lieu kenh TK6 va TK7 */
    ch6_data = TK_ReadData(6);
    ch7_data = TK_ReadData(7);

    complete = 1;
    // Clear interrupt status.
    TK_CLEAR_INTERRUPT;

    return;
}
```